# Bachelor-Thesis

## Implementation of deep learning methods on a massively parallel FPGA cluster

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**Abstract**

Deep learning frameworks continue to evolve, demanding novel approaches to achieve efficient and scalable computation. This thesis explores the integration of a specialized FPGA accelerator module, developed using VHDL, into the minimalistic deep learning framework `tinygrad`. The research addresses two key challenges: the seamless mapping of `tinygrad`'s dynamic kernel compilation model onto a specialized FPGA design, and the evaluation of scalibility within a RIVYERA S6-LX150 FPGA cluster. By designing a specialized accelerator, extending the `tinygrad` backend for hardware interfacing, and benchmarking performance against representative workloads, this work aims to provide practical insights into FPGA-based acceleration for deep learning frameworks.

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# 1 Introduction

Deep learning is rapidly evolving, with frameworks such as TensorFlow and PyTorch enabling complex model development and deployment. In contrast, tinygrad stands as a minimalistic deep learning framework implemented in only a few thousand lines of code (<12K as of 23-02-2025). Despite its simple design, tinygrad supports key features such as lazy evaluation, automatic differentiation, and operation fusion that are essential for modern deep learning workflows.

A notable characteristic of tinygrad's architecture is how it decomposes high-level operations, such as matrix multiplication, into a small set of elementary operations (e.g., ADD, MUL) that are later fused into efficient computation kernels. This approach significantly reduces the number of distinct operations requiring hardware acceleration, making tinygrad an attractive platform for experimental FPGA research and implementation.

The RIVYERA S6-LX150 presents an ideal environment for such experimentation. Our FPGA cluster contains up 40 Xilinx Spartan-6 LX150 FPGAs, its architecture offering an excellent foundation for implementing specialized accelerators for distinct neural network operations.

## 1.1 Problem Statement

The research addresses two primary challenges. First, there is the need for **operation-specific hardware design** – designing specialized FPGA implementations for critical tinygrad operations. Second, there are **integration and scalability concerns** related to seamlessly integrating a specialized FPGA accelerator module into a minimalistic deep learning framework and evaluating how the RIVYERA FPGA cluster architecture impacts scalability.

## 1.2 Objectives

This thesis aims to **design a specialized FPGA accelerator module** by implementing a set of critical operations used in tinygrad. Another key objective is to **integrate with tinygrad** by developing a custom backend – specifically a compilerthat maps tinygrad's operations onto a specialized ISA.

Additionally, the research will **deploy the specialized accelerators** across the RIVYERA S6-LX150 FPGA cluster to evaluate scalability. Finally, comprehensive **performance evaluation** will benchmark the accelerators, both as standalone modules and within the cluster configuration, using representative workloads to assess latency and throughput.

## 1.3 Research Focus and Hypotheses

The research focuses on two key questions. First, regarding integration:
**RQ1: Integration** Can specialized FPGA accelerator modules developed using VHDL be seamlessly integrated into the tinygrad framework?
**H1:** Specialized FPGA accelerator modules developed with VHDL can be integrated into the tinygrad framework with minimal code modifications and without disrupting its existing functionality. This seamless integration will maintain functional correctness and preserve the framework's ease of use, demonstrating that tinygrad's abstraction layer can effectively interface with specialized hardware accelerators.

The second question concerns scalability and cluster performance:
**RQ2: Scalability and Cluster Performance** How does deploying specialized accelerators across a RIVYERA S6-LX150 FPGA cluster affect scalability for deep learning workloads in a minimalistic framework like tinygrad?
**H2:** Deploying specialized accelerators across the RIVYERA S6-LX150 FPGA cluster will facilitate effective scalability of deep learning workloads within the tinygrad framework.

# 2 Background and Related Work

The background of this thesis encompasses the topics of deep learning frameworks, the application of FPGA clusters in this domain and the experimental equipment used.

## 2.1 Introduction to Deep Learning Frameworks and tinygrad

TensorFlow and PyTorch represent two of the most widely adopted deep learning frameworks, each with distinct design philosophies and evolving capabilities. TensorFlow, originally developed by the Google Brain Team, excels in production environments through specialized deployment tools like TensorFlow Serving, TensorFlow Lite for mobile devices, and TensorFlow.js for web applications [1].

PyTorch, developed by Facebook's AI Research lab, emphasizes dynamic computation graphs and offers native Python integration that facilitates rapid prototyping and easier debugging [18].

Tinygrad is a recent python ML framework, developed by George Hotz – initially as a personal project – in 2020, now being developed by the tiny corp startup [10]. It serves as an alternative to PyTorch and Tensorflow, putting simplicity as a key focus. Users are able to define neural networks by calling into a set of API functions to perform tensor computations. Most complex neural networks defined with tinygrad can be broken

down into an abstract syntax tree consisting of 3 types of operations - ElementwiseOps, ReduceOps, MovementOps tinygrad. [9]. Tinygrad's relative simplicity makes it an attractive framework to develop new hardware accelerators for.

## 2.2 FPGA Technology for Neural Networks

Field-Programmable Gate Arrays (FPGAs) are reconfigurable hardware, with a degree of programmability between general-purpose processors and application-specific integrated circuits (ASICs). Unlike fixed hardware, FPGAs consist of configurable logic blocks (CLBs), programmable interconnects, and dedicated resources such as block RAMs and DSP slices that enable implementation of custom computing architectures for specific applications [4].

Neural network layers perform numerous similar arithmetic operations – primarily multiply-accumulate (MAC) – that can be executed with significant parallelism. The reconfigurable logic and dedicated DSP slices of FPGAs enable designers to instantiate multiple parallel processing elements, each handling a subset of these MAC operations. Various researchers have demonstrated these parallel processing capabilities successfully in FPGA-based neural network accelerators [25].

In feed-forward neural network inference, computation typically follows a predictable dataflow pattern. Unlike general-purpose processors—which support complex instruction sets enabling arbitrary control flow (loops, recursion, dynamic memory management)—many neural network inference tasks operate with relatively static computational graphs. This more predictable structure allows FPGA implementations to be optimized specifically for the arithmetic and data movement required by the network. FPGAs can focus resources on parallel datapaths rather than complex control units [26], which can reduce power consumption and improve efficiency compared to general-purpose architectures. Multiple studies on FPGA accelerators for deep learning have confirmed these efficiency benefits [20].

Together, these aspects make FPGAs well-suited to accelerate many neural network computations by exploiting parallelism in a predictable environment—often resulting in favorable throughput, latency, and energy efficiency characteristics compared to more generalized processing architectures. It should be noted that for more complex neural network architectures involving recurrent connections or dynamic control flow, these advantages may be less pronounced, though specialized FPGA designs can still offer benefits.

## 2.3 FPGA Clusters in Deep Learning

**Uniform clusters** deploy identical FPGA devices in standardized configurations to simplify programming models and system management, enabling consistent performance characteristics across the platform. In contrast, **heterogeneous clusters** integrate diverse FPGA models with varying capabilities within a single system, tailoring specialized computational resources to different operations while potentially optimizing cost-efficiency. This architectural dichotomy was originally proposed in the Axel project [24], and as Samayoa et al. discuss in their survey, uniform systems offer simplified programming paradigms while heterogeneous systems can provide performance advantages by matching computational elements to their most suitable tasks [22].

FPGA clusters implement various communication architectures that fundamentally affect scalability, latency, and overall system performance. According to Caulfield et al. [3], there are three primary acceleration approaches: **local acceleration** (where each FPGA accelerates its own host server's workloads), **network acceleration** (where FPGAs process network flows), and **global acceleration** (where FPGAs communicate directly with each other across the datacenter to create distributed accelerator pools). Each approach offers distinct trade-offs in terms of latency, programmability, and scale.

Local acceleration connects FPGAs directly to their host processors through high-speed interfaces like PCIe or AXI, offering the lowest latency but limiting acceleration to a single node's computational capacity. Network acceleration positions FPGAs between servers and network switches to process data flows at line rates without CPU intervention. Global acceleration enables datacenter-scale FPGA communication, allowing multiple FPGAs to collaborate on workloads regardless of physical location.

The RIVYERA S6-LX150 system represents employs a PCIe-based local acceleration architecture that connects up to 128 Xilinx Spartan-6 LX150 FPGAs to create a high-performance computing cluster [23]. This architecture emphasizes tight integration through standardized PCIe interfaces rather than network-based communication, providing deterministic latency characteristics essential for specific workloads. This approach allows for low-latency communication between FPGAs within the cluster but constrains the system to a single physical enclosure.

## 2.4 Experimental Equipment - Rivyera S6-LX150

The RIVYERA S6-LX150 (as pictured in Figure 1) is a specialized FPGA-based high-performance computing platform designed for application-specific computing. The system integrates up to 128 Xilinx Spartan-6 LX150 FPGAs in a scalable architecture contained within a standard 19-inch rack-mountable 4U chassis [23].

Each FPGA in the system features 147,443 logic cells, 180 DSP48A1 slices, and 268 18Kb Block RAMs. The hardware architecture assigns 512 MB of DDR3-333 RAM to each FPGA (totaling up to 65 GB of distributed memory across the system), with optional 32 GB SDHC flash storage per FPGA.

The interconnection architecture of the RIVYERA system consists of a 16-slot backplane where each card accommodates up to 8 FPGAs. These FPGAs are connected via a high-throughput bus system that enables efficient data exchange between processing elements. The system interfaces with a host server through up to four PCIe-based interface cards, providing a bridge between the conventional computing environment and the specialized FPGA hardware.

For software development, the RIVYERA platform supports standard FPGA development workflows, including VHDL development through Xilinx ISE 14.7. The system comes with a Linux-based operating system (typically CentOS 7) and includes the SciEngines API that supports multiple design flows. This software environment facilitates both low-level hardware programming and higher-level application development, making it suitable for implementing specialized accelerators for deep learning frameworks like tinygrad.


Figure 1: Sciengines RIVYERA S6-LX150

# 3 Tinygrad Architecture

Tinygrad provides a frontend consisting of various common deep learning functions to define a chain of tensor computations. These serve to build an abstract syntax tree of operations to be carried out when a tensor's data is accessed (when the tensor is

"realized"). Realization encompasses the break-down of the abstract syntax tree into a linear list of low-level primitive operations. Each supported target device has a runtime comprising a set of classes that handle input/output and the compilation of tinygrad's low-level intermediate language into device-specific code. This analysis is based on the tinygrad codebase [9] and accompanying documentation in the tinygrad-notes repository [17].

## 3.1 Frontend

Tinygrad provides a `Tensor` class that enables users to initialize tensors and perform operations on them. Figure 2 demonstrates training a neural network using Tinygrad's API.

```python
from tinygrad import Tensor, nn

class NeuralNet:
    def __init__(self):
        self.l1 = Tensor.kaiming_uniform(784, 128)
        self.l2 = Tensor.kaiming_uniform(128, 10)
    def __call__(self, x:Tensor) -> Tensor:
        return x.flatten(1).dot(self.l1).relu().dot(self.l2)

model = NeuralNet()
optim = nn.optim.Adam([model.l1, model.l2], lr=0.001)

x, y = Tensor.rand(4, 1, 28, 28), Tensor([2,4,3,7])  # replace with real mnist dataloader

with Tensor.train():
    for i in range(10):
        optim.zero_grad()
        loss = model(x).sparse_categorical_crossentropy(y).backward()
        optim.step()
        print(i, loss.item())
```

Figure 2: Example of linear network training using Tinygrad's API

The NeuralNet model implements a two-layer feedforward network for MNIST digit classification [5]. The network accepts 28x28 grayscale images as input and produces classification outputs for ten digit classes (0-9).

The first layer (`self.l1`) consists of 128 neurons that receive flattened pixel values (784 inputs total) as shown in the `x.flatten(1).dot(self.l1)` operation. The layer outputs are processed through the ReLU activation function, defined as $ReLU(x) = \max(0, x)$, which introduces non-linearity as implemented in the `.relu()` call.

The second layer (`self.l2`) produces ten output values representing classification confidence for each digit class through the `.dot(self.l2)` operation.

The constructor initializes both layer weight matrices using Kaiming uniform initialization [6], which provides appropriate scaling for ReLU activations by drawing weights from a uniform distribution with variance adapted to the layer width.

The training loop demonstrates tinygrad's automatic differentiation capabilities. For 10 iterations, the model processes the input batch `x` to generate predictions, which are compared against ground truth labels `y` using sparse categorical cross-entropy loss. The `.backward()` call triggers automatic gradient computation through the computational graph, while the Adam optimizer [15] applies computed gradients to update model parameters via `optim.step()`. The `optim.zero_grad()` call clears accumulated gradients between iterations, ensuring proper gradient computation for subsequent steps.

### 3.1.1 Tensor initialization

The framework implements various tensor creation methods commonly used in machine learning, including `uniform` (uniform distribution sampling), `randn` (normal distribution sampling), and the previously discussed `kaiming_uniform`.

### 3.1.2 Machine Learning Operations

Common machine learning operations are implemented, including `matmul` (matrix multiplication as shown in the `.dot` operations), `layernorm` (layer normalization for training stability), and `conv2d` (2D convolution for spatial feature extraction). These operations serve as high-level abstractions and are expressed internally using primitive operations such as add and mul.

### 3.1.3 Neural Network Module

The nn module provides essential building blocks for neural networks including `Linear` (fully-connected layers), `Conv2d` (convolutional layers), and `BatchNorm` (batch normalization layers). The module also includes implementations of standard optimizers such as the previously discussed `Adam` and `SGD` (stochastic gradient descent).

### 3.1.4 Automatic Differentiation

Gradients are computed automatically using the Tensor.train() context manager and the Tensor.backward() method.

### 3.1.5 Supported Data Types

Tinygrad supports floats, integers, and booleans at various precision levels.

## 3.2 Abstract Syntax Tree

Operations are tracked within an abstract syntax tree represented by the `UOp` class. Computations remain deferred until the resulting tensor is realized through value extraction or explicit invocation of the `realize()` function.

Figure 3 demonstrates matrix multiplication performed in Tinygrad on a CUDA device.

```python
import os
os.environ["DEBUG"] = "4"  # Enables verbose logging to see UOp tree and kernels
os.environ["CUDA"] = "1"   # Forces CUDA device usage

from tinygrad import Tensor

# 1. Create two 2x2 tensors
a = Tensor([[1.0, 2.0],
[3.0, 4.0]], device="CUDA")

b = Tensor([[5.0, 6.0],
[7.0, 8.0]], device="CUDA")

# 2. Perform matrix multiplication
c = a @ b  # This is equivalent to a.matmul(b)

# 3. Realize the tensor to execute the computation
result = c.realize()
```

Figure 3: Matrix Multiplication in tinygrad

The realization of the tensor results in an abstract syntax tree consisting of operations (Figure 4) being built and executed.

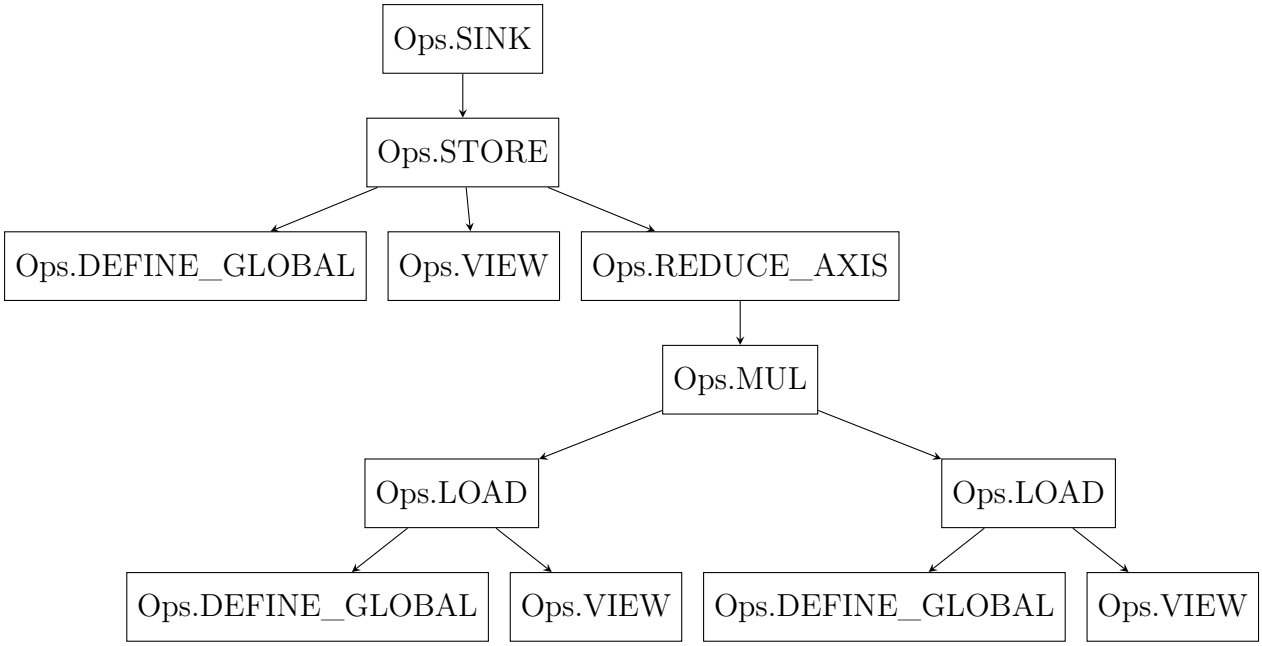



Figure 4: Matrix Multiplication Operations Tree

Looking at the graph from bottom-to-top, we see that the matrix multiplication has been broken up into an elementwise multiplication (Ops.MUL) of two same-shaped tensors followed by an axis reduction through summation (Ops.REDUCE_AXIS).

## 3.3 UOp

The Abstract Syntax Tree consists of UOp objects. These hold an identifier of the operation (i.e. Ops.MUL), a datatype (i.e. dtypes.float32), arguments (can be of any type), and a reference to source UOps it might depend on. We could not identify a definitive explanation to the naming of the UOp class in tinygrad's codebase and documentation.

## 3.4 Shape Tracker

The shape tracker is the primary component responsible for optimizing any movement/copy operations performed on a Tensor. Whenever a Tensor is defined as being a copy of another Tensor in a different shape/dimension, it is crucial to optimize such that the same memory allocated for the original tensor can be used, as opposed to copying the data.

To represent a reshaping, the Shape Tracker relies on the View class. A View possess three attributes - the Tensor it is defined over, a shape, and a stride. The shape is simply a tuple holding the size of all the dimensions of the tensor. The stride is a tuple of the same size as the shape, it defines how the memory index gets calculated for a particular element of the Tensor. For example, if we have a Tensor A with shape (4, 2) and a stride

of (4, 1) and we want to transpose it, we would define a View over with with shape (2, 4) and a stride of (1, 4).

Each Tensor has a single ShapeTracker object attached to it. The ShapeTracker simply holds a list of all the Views that define the Tensor. Whenever possible, the ShapeTracker combines several Views into one.

## 3.5 Pattern Matcher

A PatternMatcher takes a UOp matching one of its patterns and replaces it with another object. This could be another UOp in the use case of graph rewriting, or it could be a string of code as in the case of a renderer. A PatternMatcher consists of several UPat objects, that define the pattern and the object it is to be replaced with.

## 3.6 Scheduling

Each instantiated Tensor object has a corresponding, unoptimized UOp AST attached to it in the lazydata attribute. When the user reads from a Tensor (in other words - realizes the Tensor) the UOp AST stored in lazydata gets optimized, and one or more ScheduleItem get created, which then get executed in order to perform the computation and finish the realization of the tensor. The process of creating the ScheduleItems is called Scheduling. The Grouper component determines which operations in the AST get performed in their own ScheduleItem, and simplifies/optimizes the AST. It does using several different PatternMatchers, which match particular elements of the AST and replace them with an optimized counterpart.

**Schedule Item** A schedule item represents a single UOp AST that is to be executed. It consists of an ast attribute holding the UOp AST, and a bufs attribute, which is a list of Buffer objects that are to be used for the computation.

## 3.7 Graph Rewrite

Graph rewrite refers to all transformations performed on a UOp computational graph during realization.

### 3.7.1 Grouper

The first graph rewrites of the AST that take place during scheduling are handled by the grouper component. Optimizations and preparations of the AST to be rendered to the target device take place. Operations get fused and simplified where possible and intermediate OPs are replaced with their counterparts. It is at this stage, where the AST potentially gets broken up into separately rendered kernels.

### 3.7.2 Lowering to SIMT

In parallel computing, Single instruction, multiple threads (SIMT) is an execution model introduced by NVIDIA [16], whereby a single instruction is executed on a multitude of threads in parallel to achieve a high computational bandwidth. This is the primary model employed by most modern GPUs. CUDA Kernels, for example, are programs that process some portion of input data, with the particular portion to be processed being determined by the identifier of the thread. These kernels are executed on several threads synchronously, such that a large amount of input data may be processed at once.

SIMT is widely employed in deep learning computations, and a majority of accelerators implement this paradigm in their programming frontends. Correspondingly, Tinygrad implements the process of "Lowering", which is aimed at breaking down high-level vector operations into a series of lower-level primitive operations that are to be executed across several threads.

It is the final stage of graph rewriting for the AST broken down into a linear list of primitive UOps (linearization) that can be rendered into code for a SIMT-compatible device.

## 3.8 Runtime

After the UOp AST is built, it is passed to the specific device backend (e.g. CUDA Backend, CPU Backend) for execution. Figure 5 displays the components of the CUDA Backend.

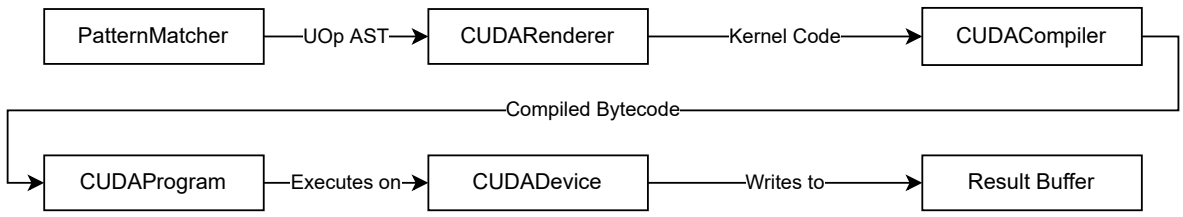



Figure 5: CUDA Backend Processing Pipeline in tinygrad

Tinygrad was designed with execution on NVIDIA and AMD GPUs in mind. These have their own C++-based programming frontends (CUDA and ROCm respectively). A significant part of tinygrad's architecture is designed around rendering the UOp AST to C++ code, and then compiling this C++ to a binary that can be executed on the accelerator device. The Renderer component is responsible for outputting a string containing the C++ code that performs the computation defined by the UOp.

Since we are developing an FPGA Accelerator specifically for tinygrad, it simplifies the development of the Backend significantly. We intend to use tinygrad as our only programming frontend, allowing us to design our accelerator around tinygrad's native UOp AST, simplifying the renderer and compiler as opposed to having to work with an additional programming frontend in between.

# 4 System Design and Implementation

This section presents the integrated design of specialized FPGA accelerator modules for tinygrad operations, their deployment across the RIVYERA S6-LX150 cluster, and the mapping strategy that connects tinygrad's abstract operations to hardware implementations. The design philosophy prioritizes functional correctness and integration feasibility over optimal performance, creating a reference implementation that demonstrates the viability of tinygrad-FPGA integration.

## 4.1 Design Philosophy and Constraints

This work adopts a **reference implementation** strategy that prioritizes:

- **Integration feasibility**: Demonstrating successful mapping of tinygrad operations to FPGA hardware
- **Scalability validation**: Characterizing performance scaling across multiple FPGAs
- **Correctness verification**: Ensuring functional equivalence with existing tinygrad backends
- **Implementation clarity**: Employing established architectural patterns that demonstrate integration principles

This approach focuses development effort on the core research questions (RQ1: Integration and RQ2: Scalability) while establishing a foundation for future optimization work.

### 4.1.1 RIVYERA S6-LX150 Resource Constraints

The Xilinx Spartan-6 LX150 FPGAs impose specific design constraints:

- **Logic Resources**: 147,443 logic cells per FPGA requiring careful resource allocation
- **DSP Capabilities**: 180 DSP48A1 slices per FPGA providing dedicated multiply-accumulate functionality

- **Memory Resources**: 268 18Kb Block RAMs (4.8 MB total) plus 512 MB DDR3 per FPGA
- **Communication**: High-throughput bus system between FPGAs with PCIe host interface

These constraints necessitate architectures that balance resource utilization with implementation complexity, favoring proven designs over experimental optimizations.

## 4.2 VHDL Development Fundamentals

VHDL, defined by IEEE 1076 [12], is a hardware description language used for ASIC and FPGA development. Unlike traditional programming languages that define sequential instructions for Turing-complete machines, VHDL specifies physical signal connections [2]. Signal assignment occurs concurrently in parallel, making VHDL particularly suitable for massively parallel computing implementations.

For example, a simple 32-bit adder (Figure 6):

```vhdl
entity adder is
    port (
        a     : in  std_logic_vector(31 downto 0);
        b     : in  std_logic_vector(31 downto 0);
        sum   : out std_logic_vector(31 downto 0)
    );
end entity adder;

architecture concurrent of adder is
begin
    sum <= std_logic_vector(unsigned(a) + unsigned(b));
end architecture concurrent;
```

Figure 6: VHDL Implementation of a 32-bit adder

This single concurrent assignment continuously computes the sum whenever inputs `a` or `b` change, showing how VHDL models hardware behavior rather than sequential execution.

While concurrent signal assignments form the foundation of VHDL design, many hardware components require sequential behavior. VHDL addresses this through processes - blocks of code that execute sequentially when triggered by specific signal changes. These processes enable the implementation of state machines, control logic, and other sequential circuits that are essential for our pipeline stages.

Consider a simple counter that increments on each clock cycle (Figure 7) - this cannot be implemented with concurrent assignments alone:

```vhdl
entity counter is
    port (
        clk    : in  std_logic;
        rst    : in  std_logic;
        enable : in  std_logic;
        count  : out std_logic_vector(31 downto 0)
    );
end entity counter;

architecture sequential of counter is
    signal count_reg : unsigned(31 downto 0) := (others => '0');
begin
    process(clk)
    begin
        if rising_edge(clk) then
            if rst = '1' then
                count_reg <= (others => '0');
            elsif enable = '1' then
                count_reg <= count_reg + 1;  -- Depends on previous value
            end if;
        end if;
    end process;

    count <= std_logic_vector(count_reg);
end architecture sequential;
```

Figure 7: VHDL Implementation of a counter

The counter must remember its previous value between clock cycles, requiring a clocked process to implement this stateful behavior.

Building on signals and processes, we can construct pipelined architectures - a design pattern fundamental to achieving high throughput in FPGA implementations [14]. When a calculation becomes too long to complete within one clock cycle, it must be broken into smaller stages and completed over several clock cycles.

Consider a simple example: computing `a <= b + c + d`. Without pipelining (Figure 8), this requires two additions in series:

```vhdl
-- Non-pipelined version
process(clk)
begin
    if rising_edge(clk) then
        a <= b + c + d;  -- Two additions in one cycle
    end if;
end process;
```

Figure 8: VHDL Implementation of addition without pipelining

To pipeline this operation, we introduce an intermediate register to separate the additions (Figure 9):

```vhdl
-- Pipelined version
signal temp : std_logic_vector(31 downto 0);  -- Pipeline register

process(clk)
begin
    if rising_edge(clk) then
        -- Stage 1: First addition
        temp <= b + c;

        -- Stage 2: Second addition
        a <= temp + d;
    end if;
end process;
```

Figure 9: VHDL Implementation of addition with pipelining

This design completes one full addition every clock cycle after an initial latency of two cycles.

## 4.3 Tinygrad Operation Analysis and Hardware Mapping

Analysis of tinygrad's linearization process reveals that only a subset of operations reach the final optimized AST for code generation and device compilation. The linearized UOp list contains primitive operations after all high-level transformations and optimizations. Operations reaching hardware implementation fall into five categories:

**Memory Management Operations** These operations handle memory allocation, access patterns, and data movement:

- **DEFINE_GLOBAL**: Declares global memory buffer pointers with specified data types and sizes
- **DEFINE_LOCAL**: Declares local/shared memory buffers for thread-group communication
- **LOAD**: Memory read operations with optional gating for conditional execution
- **STORE**: Memory write operations to global or local memory spaces
- **INDEX**: Address calculation and pointer arithmetic for memory access

**Arithmetic and Logic Unit (ALU) Operations** The core computational operations are grouped into three subcategories based on operand count:

**Unary Operations:**

- **CAST/BITCAST**: Type conversion between different data formats
- **NEG**: Arithmetic negation
- **RECIP**: Reciprocal calculation ($1/x$)
- **SQRT**: Square root function
- **EXP2/LOG2**: Exponential and logarithmic functions (base 2)
- **SIN**: Trigonometric sine function

**Binary Operations:**

- **ADD/SUB**: Addition and subtraction
- **MUL**: Multiplication
- **FDIV/IDIV**: Floating-point and integer division
- **MOD**: Modulo operation
- **MAX**: Maximum selection
- **CMPLT/CMPNE**: Comparison operations (less than, not equal)
- **AND/OR/XOR**: Bitwise logical operations
- **SHL/SHR**: Bit shift operations (left/right)
- **POW**: Power function

**Ternary Operations:**

- **WHERE**: Conditional selection ($c?a : b$)

- **MULACC**: Multiply-accumulate operation ($a \times b + c$)

**Control Flow Operations** These operations implement structured control flow within kernels:

- **RANGE**: Loop initialization with start/end bounds and iteration variable
- **ENDRANGE**: Loop termination and iterator increment
- **IF**: Conditional block entry based on predicate evaluation
- **ENDIF**: Conditional block exit
- **BARRIER**: Thread synchronization primitive for coordinated execution

**Data Flow Operations** Operations that manage data dependencies and accumulator patterns:

- **DEFINE_ACC**: Accumulator initialization with specified data type and initial value
- **ASSIGN**: Assignment operation for updating accumulator values
- **CONST/VCONST**: Constant value definitions (scalar and vector)

This operation set forms the foundation for our accelerator ISA design, requiring approximately 50 distinct instruction types to implement the complete tinygrad execution model.

## 4.4 Accelerator Architecture

Due to tinygrad's SIMT focus, we implement a multi-core system with a RISC-V-like ISA (described in Tables 1 and 2), executing kernels across multiple cores in parallel, similar to GPU architectures. Our architecture adapts open-source RISC-V FPGA implementations [27], modifying cores to maintain individual register files while sharing memory across the system. This simplified model introduces performance and scalability limitations discussed in the Discussion section.

Table 1: Rivyera Accelerator Instruction Formats

| Type | 31-26 | 25-21 | 20-16 | 15-11 | 15-0 |
|---|---|---|---|---|---|
| R-type | opcode[5:0] | rd[4:0] | rs1[4:0] | rs2[4:0] | - |
| I-type | opcode[5:0] | rd[4:0] | - | - | immediate[15:0] |
| M-type | opcode[5:0] | rd[4:0] | rs1[4:0] | - | immediate[15:0] |
| J-type | opcode[5:0] | - | rs1[4:0] | - | immediate[15:0] |

Table 2: Rivyera Accelerator Instruction Set

| Instruction | Opcode | Type | Description |
|---|---|---|---|
| ADD | 000001 | R-type | rd = rs1 + rs2 (integer) |
| SUB | 000010 | R-type | rd = rs1 - rs2 (integer) |
| MUL | 000011 | R-type | rd = rs1 × rs2 (integer) |
| DIV | 000100 | R-type | rd = rs1 ÷ rs2 (integer) |
| MOD | 000101 | R-type | rd = rs1 mod rs2 |
| SHL | 000110 | R-type | rd = rs1 << rs2 |
| SHR | 000111 | R-type | rd = rs1 >> rs2 |
| AND | 001000 | R-type | rd = rs1 ∧ rs2 |
| OR | 001001 | R-type | rd = rs1 ∨ rs2 |
| XOR | 001010 | R-type | rd = rs1 ⊕ rs2 |
| NEG | 001011 | R-type | rd = -rs1 (integer) |
| CMPLT | 001100 | R-type | rd = (rs1 < rs2) ? 1 : 0 (integer) |
| CMPNE | 001101 | R-type | rd = (rs1 ≠ rs2) ? 1 : 0 (integer) |
| MAX | 001110 | R-type | rd = max(rs1, rs2) (integer) |
| MOV | 010000 | R-type | rd = rs1 |
| LOAD_IMM | 010001 | I-type | rd = immediate |
| FADD | 010010 | R-type | rd = rs1 + rs2 (float) |
| FSUB | 010011 | R-type | rd = rs1 - rs2 (float) |
| FMUL | 010100 | R-type | rd = rs1 × rs2 (float) |
| FDIV | 010101 | R-type | rd = rs1 ÷ rs2 (float) |
| FSQRT | 010110 | R-type | rd = sqrt(rs1) |
| FRECIP | 010111 | R-type | rd = 1/rs1 |
| FMAX | 011010 | R-type | rd = max(rs1, rs2) (float) |
| FNEG | 011011 | R-type | rd = -rs1 (float) |
| FNE | 011100 | R-type | rd = (rs1 ≠ rs2) ? 1 : 0 (float) |
| FLT | 011101 | R-type | rd = (rs1 < rs2) ? 1 : 0 (float) |
| FTOI | 011110 | R-type | rd = (int)rs1 (float to signed int) |
| FTOUI | 011111 | R-type | rd = (uint)rs1 (float to unsigned int) |
| ITOF | 100010 | R-type | rd = (float)rs1 (signed int to float) |
| UITOF | 100011 | R-type | rd = (float)rs1 (unsigned int to float) |
| LOAD | 100000 | M-type | rd = memory[rs1 + immediate] |
| STORE | 100001 | M-type | memory[rs1 + immediate] = rd |
| JMP | 110000 | J-type | PC = target |
| JZ | 110001 | J-type | if (rs1 = 0) PC = target |
| JNZ | 110010 | J-type | if (rs1 ≠ 0) PC = target |
| HALT | 111101 | R-type | Stop execution |
| BARRIER | 111110 | R-type | Synchronization barrier |
| NOP | 111111 | R-type | No operation |

R-type instructions comprise binary and unary operations (e.g., ADD, MUL, NEG) that compute values from up to two source registers (rs1 and rs2) and store results in the destination register (rd).

The only I-type instruction is LOAD_IMM, which stores the 16-bit immediate value into the destination register (rd).

M-type instructions are STORE and LOAD. The STORE operation writes the value in rd to shared memory at address rs1 + immediate, while LOAD reads from address rs1 + immediate and stores the retrieved value in rd.

J-type instructions include JMP, JZ, and JNZ. These instructions branch to target ad-

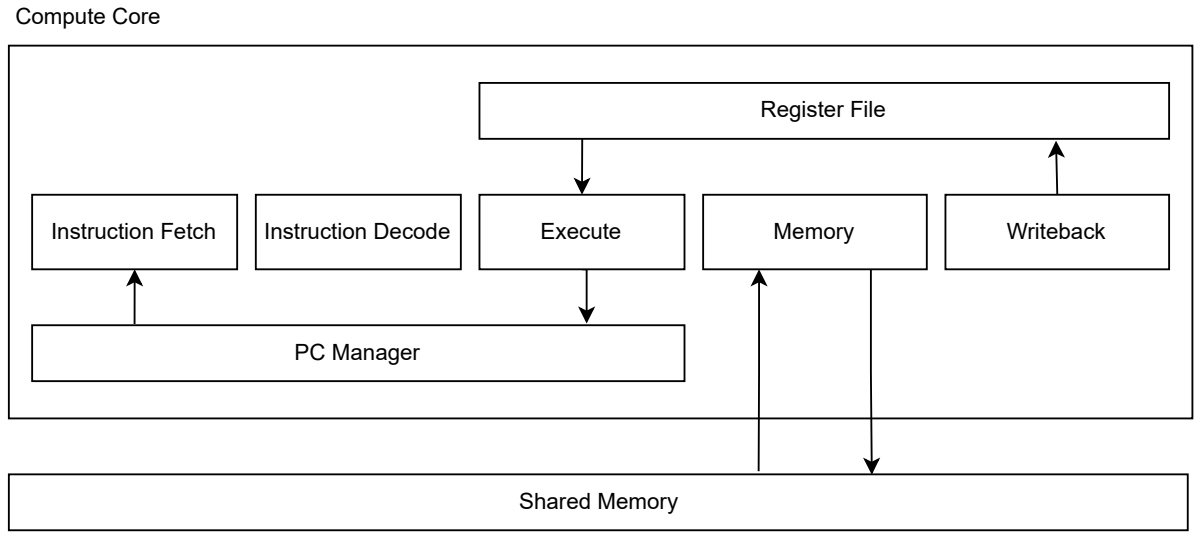
dresses calculated by adding the immediate value to the current program counter, with JZ and JNZ performing conditional branches based on whether rs1 equals zero.

**Precision and Implementation Considerations** The floating-point unit implements IEEE 754 single-precision format as the primary data type, with provisions for future half-precision extensions commonly used in neural networks.

### 4.4.1 Compute Core Architecture

The implementation follows the classic five-stage RISC pipeline: Instruction Fetch, Instruction Decode, Execute, Memory, and Writeback [8]. Core components implement each pipeline stage.

Figure 10: Compute Core Architecture




Instructions reside in BRAMs within the Instruction Fetch component, loadable through an external interface extending to the top-level host interface. The PC Manager stores and updates the program counter, accepting inputs from the execution engine for jump operations. The Memory Stage provides an external interface for global memory read/write operations.

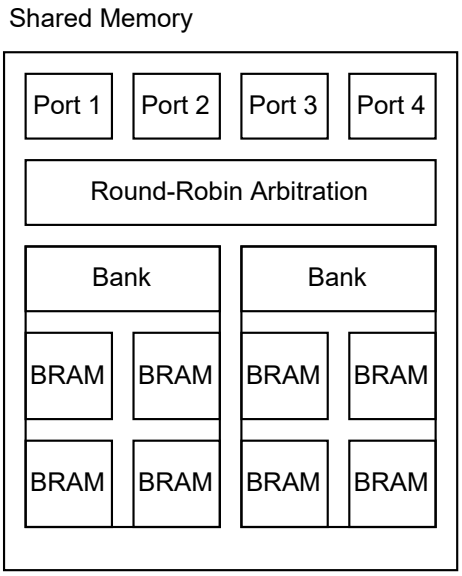
### 4.4.2 Arithmetic Logic Unit

The ALU performs both integer and floating-point arithmetic operations. Integer and logical operations utilize integrated VHDL operators. Floating-point operations employ the 2008 VHDL Standard Library implementation of IEEE 754 single-precision arithmetic [12].

### 4.4.3 Shared Memory

BRAM arrays organize into memory banks with arbitrated access ports. The maximum concurrent operations equals the number of memory banks. Access conflicts resolve through round-robin arbitration [13].

Figure 11: Shared Memory



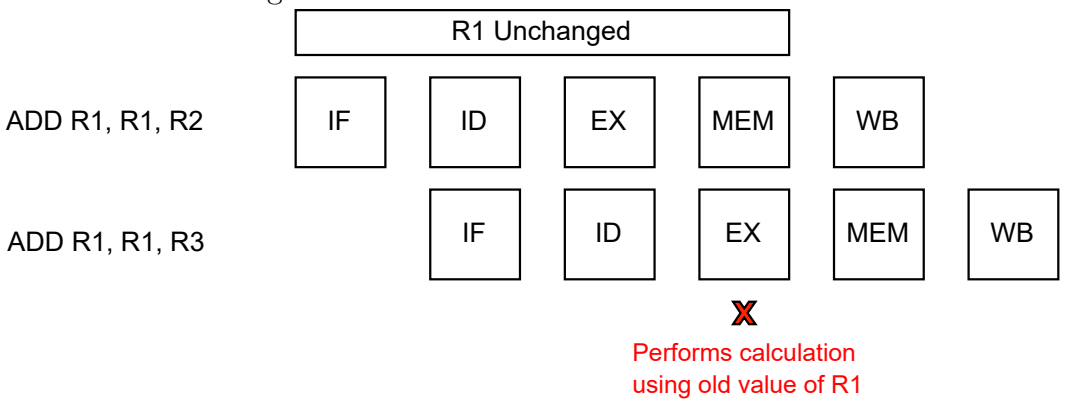

### 4.4.4 Pipeline Hazard Management

Pipeline hazards occur when pipeline stages would produce incorrect results, typically due to dependencies on uncompleted previous instructions [8].

A typical example is a Read-After-Write (RAW) data hazard:

```
1 ADD R1, R1, R2
2 ADD R1, R1, R3
```

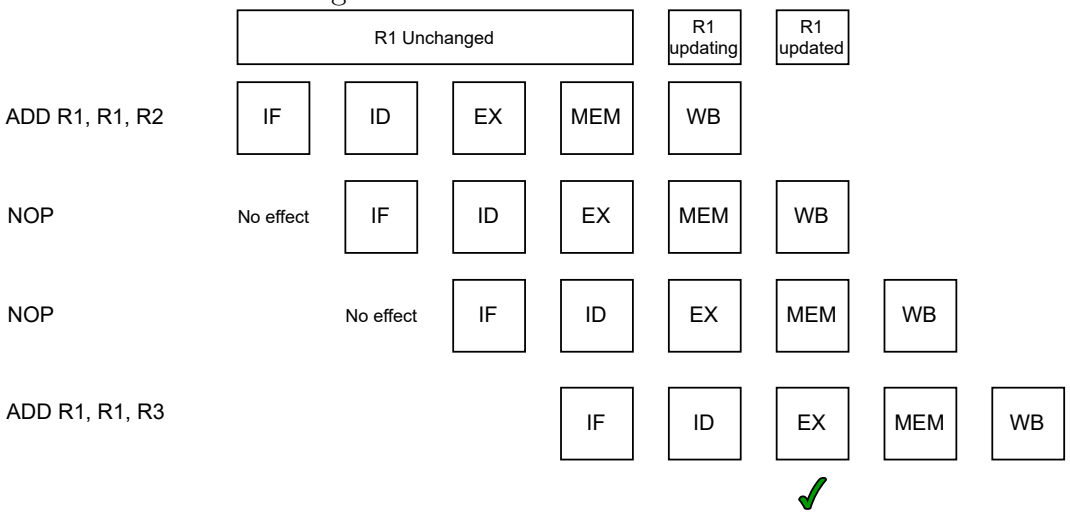
Figure 12: Read-After-Write data hazard



Without hazard handling, the pipeline would execute incorrectly. The execution stage of the second instruction depends on the writeback stage of the first instruction completing. However, when the second instruction's execution stage runs, the first instruction has only reached the memory stage. Thus, R1 would not be updated before the second instruction reads it.

Our implementation resolves hazards by detecting them during assembly and inserting NOP operations to stall the pipeline.

Figure 13: Resolved data hazard




This approach impacts performance through wasted computational cycles. While forwarding techniques can resolve such hazards more efficiently [11], our reference implementation prioritizes simplicity over optimization.

## 4.5 Host-FPGA Communication

The Sciengines C-API provides host-FPGA communication functionality. Python bindings generated via clang2py [7] enable FPGA programming and memory operations from Python code.

## 4.6 Compiler Design

The RivyeraCompiler translates tinygrad's linearized UOp list directly into our FPGA's native instruction set. Each UOp operation maps to one or more ISA instructions, with the compiler selecting the appropriate opcode based on data type. For example, an ADD operation on floating-point tensors generates an FADD instruction (opcode 0x12), while integer addition uses the ADD instruction (opcode 0x01). This type-aware translation ensures operations execute correctly on the appropriate hardware units within each compute core.

Register allocation follows the linear scan algorithm [19], using 24 general-purpose registers (r6 through r29). Registers r0-r5 are reserved for special purposes, r30 stores the spill memory base address, and r31 contains the thread ID. UOps resulting in a computed value get assigned a register. When registers are exhausted, the compiler assigns a location in spill memory. Each core has dedicated spill memory located at the high end of the address space.

Our pipeline implementation requires careful handling of data dependencies between instructions. The compiler detects Read-After-Write (RAW) hazards by tracking when each register becomes available for reading. Currently, we employ a conservative approach that inserts 5 NOP instructions between dependent operations. While this simplifies implementation and guarantees correctness, it reduces performance compared to more sophisticated techniques like forwarding. Branch instructions require additional handling since they flush the pipeline. The compiler automatically inserts 2 NOPs after each branch to account for instructions that may have been fetched but should not execute.

The compiler generates a binary format designed for runtime patching. Each compiled kernel begins with a header containing a magic number (0xDEADBEEF) followed by placeholder information. Buffer addresses cannot be determined at compile time since they depend on runtime memory allocation. The compiler generates placeholder instructions that are patched with actual addresses before execution. The main instruction stream follows the header, with each instruction encoded as a 32-bit word matching our VHDL instruction formats. This approach allows the same compiled kernel to work with different buffer allocations across multiple executions.

Control flow operations like loops require special handling to map tinygrad's high-level constructs to basic jump instructions. The RANGE UOp initiates allocates a counter register and initializes it to zero. The loop starts with comparing the counter register against the limit, and conditionally jumping to after the loop end. At the corresponding ENDRANGE, the compiler generates an instruction to increment the counter and an unconditional jump back to the loop start. Jump targets use a label-based system where the compiler records label positions during the first pass and patches jump instructions with actual addresses in a second pass. This two-pass approach supports arbitrary control flow patterns including nested loops and conditional execution blocks.

## 4.7 Cluster Architecture

The implementation utilizes tinygrad's multi-device inference support, creating a horizontal cluster that processes multiple inputs across multiple FPGAs in parallel. The architecture does not support vertical parallelism – FPGAs cannot combine memory resources for larger models or computational resources for reduced latency – but achieves

higher throughput through horizontal scaling.

## 4.8 Verification and Testing Strategy

**VHDL-Level Tests** Functionality verification employs testbenches with the Xilinx ISim simulator, including:

- Unit tests for individual modules (ALU, Instruction Fetch component)
- Integration tests for interacting components (Multi-Core system)

**System-Level Integration Tests** Python unit tests verify end-to-end functionality, testing both host code and simulated VHDL accelerator behavior.

## 4.9 Integration with Tinygrad Backend

The tinygrad backend implementation comprises four components: RivyeraDevice, RivyeraAllocator, RivyeraRenderer, and RivyeraCompiler.

Tinygrad processes computations through the following pipeline:

1. Linearized UOps pass through RivyeraRenderer to RivyeraCompiler
2. RivyeraRenderer forwards UOps directly to RivyeraCompiler for binary compilation
3. RivyeraAllocator (instantiated within RivyeraDevice) handles buffer allocation and I/O
4. The compiled kernel executes via RivyeraDevice's ___call___ method

Certain properties of the RivyeraRenderer class determine how tinygrad groups and lowers operations. The has_local attribute determines whether the device supports SIMT execution. When enabled, RANGE operations are flattened, with each iteration executed on a separate thread.

We initially intended to utilize SIMT on our accelerator, but discovered that the number of threads required by the accelerator device scales with the dimensions of the tensor computation. This requires a very high number of threads to support the majority of deep learning workloads. While this could have been feasible with an architecture that allows a high number of virtual cores, our architecture supports only one logical thread per physical compute core. Therefore, while our architecture fundamentally supports SIMT, we cannot integrate it with tinygrad's SIMT capabilities.

### 4.10 Selection of Parameters

The primary parameters of our architecture are the number of compute cores and the number of banks and BRAMs per bank in the shared memory component. Since we cannot use SIMT as discussed previously, we configure the system with only one compute core. For the shared memory component, we use two banks (sufficient to service the single compute core and the external memory interface) with 120 BRAMs per bank to fully utilize all BRAMs available on the FPGA.

## 5 Evaluation Methodology

### 5.1 Benchmark Selection

We select tinygrad's ConvNet implementation for MNIST dataset classification as our benchmark workload. This model comprises 8 convolutional and fully-connected layers (2x Conv2d-ReLU blocks followed by BatchNorm2d and MaxPool2d, repeated twice, then a linear classifier) with approximately 600K parameters.

### 5.2 Performance Metrics

We adopt the performance metrics established by the MLPerf Inference benchmark suite [21] and measure three primary metrics:

- **Single-device inference latency**: End-to-end time for single-sample classification, measured as the 90th-percentile latency over 1,024 queries after model warm-up, following MLPerf's single-stream scenario [21]
- **Single-device inference throughput**: Maximum samples processed per second on a single FPGA device, measured using MLPerf's offline scenario methodology with a batch of at least 24,576 samples [21]
- **Multi-device inference throughput**: Aggregate samples per second across all 40 FPGA devices, measured by distributing batches across devices and summing individual throughputs

All measurements exclude one-time costs (model loading, compilation) and report median values over 100 runs to ensure statistical validity, consistent with MLPerf's requirement for measuring steady-state behavior [21].

### 5.3 Experimental Setup

- **Hardware**: 40 Spartan 6-LX150 FPGA-devices on the Sciengines Rivyera server [23]

– **Software**: Tinygrad (Revision number: 218e01833dd81586cec37f1684d5f5795072ee9b) with JIT compilation disabled, batch size of 512 samples

Target accuracy threshold is set at 98% on MNIST test set to ensure functional correctness alongside performance evaluation.

### 5.4 Measurement Procedure

Following the MLPerf Inference benchmark methodology [21], our measurement procedure consists of:

1. **Warm-up phase**: Execute 10 inference iterations to ensure steady-state operation and allow FPGA thermal equilibrium
2. **Latency measurement**:
   - Submit 1,024 sequential queries with single samples
   - Record end-to-end inference time for each query
   - Report 90th-percentile latency as the primary metric
3. **Throughput measurement**:
   - Submit batches of 512 samples continuously for 60 seconds minimum
   - Process at least 24,576 total samples per run
   - Calculate throughput as total samples divided by total time
4. **Multi-device scaling**:
   - Distribute inference workload across N devices (N = 1, 2, 4, 8, 16, 32, 40)
   - Measure aggregate throughput as sum of individual device throughputs
   - Calculate scaling efficiency relative to single-device performance

Each measurement is repeated 100 times, with the median value reported to minimize impact of outliers, following MLPerf's guidance on statistical robustness [21].

## 6 Results and Analysis

**FPGA Implementation** We were unable to generate a working FPGA implementation for our design due to failing timing constraints caused by excessive combinational logic levels in the ALU component, as documented in the timing report in Appendix D. Consequently, we could not perform the planned benchmarks on the cluster.

**Functional Correctness** Despite the inability to deploy the design on the physical FPGA cluster, we confirmed functional correctness of the system using the Sciengines simulation environment through tests performing basic matrix multiplication operations, as detailed in Appendix C.

**User experience and programmability** The accelerator integrates with the framework through a standard interface, enabling users to describe neural network workloads using the Tinygrad frontend. Device selection requires only setting an environment variable to specify the Rivyera platform.

**Limitations and constraints** The accelerator's memory architecture cannot exceed 512KB through vertical scaling, restricting compatible workloads to those within this memory footprint. The following floating-point operations are not implemented in the current design: sine, cosine, exp2, and log2. Models requiring these operations cannot be executed on this platform.

# 7 Discussion

This section analyzes the outcomes of our attempt to integrate Tinygrad with custom FPGA accelerators through a RISC-V-inspired architecture deployed on the RIVYERA S6-LX150 cluster. While the implementation achieved functional correctness in simulation and successfully demonstrated the mapping of Tinygrad's primitive operations to hardware, critical timing constraint violations prevented deployment on physical FPGAs, limiting our ability to fully validate the proposed hypotheses.

## 7.1 Key Findings and Insights

The implementation demonstrates partial success in addressing the research questions. While we achieved functional correctness through simulation and successfully integrated Tinygrad operations with FPGA hardware at the architectural level, the inability to generate a working FPGA bitstream due to timing constraint violations prevented full experimental validation.

**Addressing RQ1 (Integration)**: The research successfully demonstrated that Tinygrad's primitive operations can be mapped to a RISC-V-inspired FPGA architecture. The compiler successfully translates Tinygrad's UOp AST to assembly instructions, and simulation results confirm functional correctness for basic matrix multiplication operations. However, the hypothesis (H1) regarding seamless integration could not be fully validated due to the implementation challenges with the combinational ALU design.

**Addressing RQ2 (Scalability)**: Without a working FPGA implementation, we could not evaluate the scalability across the RIVYERA cluster. The theoretical architecture supports multi-device deployment through Tinygrad's existing multi-accelerator framework, but hypothesis (H2) remains unverified.

## 7.2 Design Tradeoffs and Decisions

The architecture prioritizes implementation simplicity and integration reliability over raw performance metrics. This design philosophy guided several key decisions: the scalar ALU architecture minimizes verification complexity compared to vector designs, the fixed 512KB memory eliminates complex memory management logic, and the direct mapping of Tinygrad operations to RISC-V instructions reduces the compiler complexity. These choices facilitate rapid prototyping and reduce potential sources of integration errors, aligning with the primary goal of demonstrating framework-accelerator integration.

**Critical Design Flaw**: The single-cycle combinational ALU implementation proved to be the primary obstacle. The timing analysis revealed excessive combinational logic levels that violated the Spartan-6 FPGA's timing constraints. A multi-cycle pipelined ALU design would have addressed this issue by distributing the computational logic across multiple clock cycles, reducing the critical path length and enabling successful synthesis.

Several architectural alternatives were evaluated during the design phase:

**Memory architecture**: DDR3 memory integration would provide orders of magnitude higher capacity compared to the current 512KB BRAM limitation. However, this would require complex memory controllers and introduce variable latency that complicates the execution model.

**Computational units**: SIMD vectorized operations, common in contemporary accelerators, would increase throughput by processing multiple data elements simultaneously. The current scalar approach trades this performance benefit for reduced control logic complexity.

**Scaling strategies**: Inter-FPGA communication protocols could enable model weight distribution across multiple accelerators, overcoming the 512KB memory limitation of individual devices. This approach would partition large models across the FPGA cluster, with each device storing a subset of weights and intermediate activations. Implementation would require synchronization mechanisms for coordinating computation phases and high-bandwidth interconnects for transferring activations between pipeline stages.

**Tensor processing units**: Dedicated matrix multiplication circuits could accelerate common operations. Tinygrad's architecture supports such extensions, but implementation would significantly increase design complexity.

**Design methodology**: Systematic design space exploration using automated tools could optimize the architecture parameters. The current manual approach prioritized rapid iteration over exhaustive optimization.

**Dynamic reconfiguration**: Runtime bitstream generation based on specific Tinygrad kernels could optimize resource usage for each workload. However, FPGA synthesis times (typically hours) make this approach impractical for dynamic workloads.

## 7.3 Limitations and Challenges

### Technical limitations encountered

The current implementation faces several critical constraints:

- **Timing closure failure**: The combinational ALU exceeded timing constraints on the Spartan-6 FPGA, preventing bitstream generation
- **Pipeline inefficiency**: The five-stage pipeline relies exclusively on NOP insertion for hazard resolution, introducing unnecessary stalls
- **Memory bandwidth limitations**: Restrict data movement between the accelerator and host system
- **Missing operations**: Absence of transcendental functions (sin, cos, exp2, log2) limits model compatibility

### Areas for improvement

A revised architecture addressing the timing closure issue would require:

- **Multi-cycle ALU**: Implementing a pipelined ALU that distributes floating-point operations across multiple clock cycles
- **Pipeline enhancements**: Dynamic hazard detection and forwarding paths to reduce NOP insertion overhead
- **Memory hierarchy**: Prefetching mechanisms and cache structures to improve data access patterns
- **Compiler optimizations**: Sophisticated instruction scheduling to minimize pipeline stalls and better utilize hardware resources

### Unresolved issues

The inability to deploy on physical hardware leaves several questions unanswered:

- Actual performance characteristics compared to CPU/GPU implementations
- Scaling efficiency across multiple FPGAs in the cluster

- Real-world bottlenecks in the host-FPGA communication interface

# 8 Conclusion and Future Work

This research investigated the feasibility of integrating the Tinygrad deep learning framework with specialized FPGA accelerators, seeking to demonstrate both seamless framework integration and cluster scalability. Although timing closure failures prevented physical deployment and empirical validation, the work establishes groundwork for framework-accelerator integration and identifies key architectural considerations for future FPGA-based deep learning implementations

## 8.1 Conclusion

This work explores the feasibility of integrating the Tinygrad framework with custom FPGA accelerators through a minimal RISC-V-inspired architecture. While the implementation successfully demonstrates the conceptual mapping of Tinygrad's primitive operations to hardware and validates the framework's potential for FPGA deployment, the inability to achieve timing closure on the Spartan-6 FPGA prevented empirical validation of our hypotheses.

The research provides valuable insights into the challenges of FPGA-based deep learning acceleration:

1. **Architectural simplicity vs. timing constraints**: The single-cycle combinational ALU, while conceptually simple, proved incompatible with FPGA timing requirements
2. **Framework integration feasibility**: Tinygrad's minimal operation set successfully maps to RISC-V-like instructions, validating the framework's suitability for hardware acceleration

Despite not achieving a working FPGA implementation, this project establishes groundwork for future framework-accelerator integration efforts and identifies critical design considerations for FPGA-based deep learning accelerators.

## 8.2 Future Work

Three primary directions emerge for extending this work:

**Immediate architectural revision**: The most critical next step involves redesigning the ALU as a multi-cycle pipelined unit. This would distribute the floating-point computation logic across multiple pipeline stages, ensuring timing closure on the target FPGA.

**Performance optimization**: Following successful FPGA deployment, optimizations should focus on:

- Pipeline forwarding mechanisms to reduce data hazards
- SIMD operations for parallel data processing
- Improved memory access patterns
- Dynamic instruction scheduling in the compiler

**Scaling mechanisms**: Developing inter-FPGA communication protocols to enable model partitioning across multiple devices, addressing the 512KB memory constraint. This includes:

- High-bandwidth interconnects between FPGAs
- Distributed memory management for model weights
- Synchronization protocols for coordinated computation
- Load balancing strategies across the cluster

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# Overview of Tools Used

This thesis was prepared with the assistance of Anthropic's Claude AI assistant in the following capacities:

**Research and Writing Assistance:**

- Section 1 – Introduction
- Section 2 – Background and Related Work
- Section 4 – System Design and Implementation
- Section 5 – Evaluation Methodology
- Section 6 – Results and Analysis
- Section 7 – Discussion
- Section 8 – Conclusion

**Code Implementation:**

- VHDL hardware descriptions provided in the appendices
- Python backend integration code for tinygrad

**Editorial Support:**

- Grammar correction and stylistic guidance throughout the thesis
- Academic writing standards and formatting assistance

# A Appendix A: Detailed VHDL Implementation

## A.1 Top-Level Module Implementation

```
---
-- Project: rivyera-accelerator
-- File:    rivyera_accelerator_main.vhd
-- Description: Top level module for rivyera accelerator
---
library ieee;
use work.sciengines_api_types.all;
use ieee.STD_LOGIC_1164.all;
```

```
9  use ieee.numeric_std.all;
10 use work.types_pkg.all;
11 use work.isa_pkg.all;
12 use work.shared_memory_types.all;
13
14 library UNISIM;
15 use UNISIM.VComponents.all;
16
17 entity rivyera_accelerator_main is
18    generic (
19       NUM_LEDS : integer
20    );
21    port (
22       -- API PORTS
23       api_clk_in        : in    std_logic;
24       api_rst_in        : in    std_logic;
25       api_led_out       : out   seBusFlag_type(NUM_LEDS-1 downto 0) := (others => '0');
26       api_hw_rev_in     : in    seHwRev_type;
27       -- ADDRESS PORTS
28       api_self_contr_in : in    seFlag_type;
29       api_next_contr_in : in    seSlotAddr_type;
30       api_prev_contr_in : in    seSlotAddr_type;
31       api_self_slot_in  : in    seSlotAddr_type;
32       api_self_fpga_in  : in    seFpgaAddr_type;
33       -- OUTPUT REGISTER PORTS
34       api_o_clk_out     : out   std_logic;
35       api_o_rfd_in      : in    seFlag_type;
36       api_o_tgt_slot_out: out   seSlotAddr_type := (others => '0');
37       api_o_tgt_fpga_out: out   seFpgaAddr_type := (others => '0');
38       api_o_tgt_reg_out : out   seRegAddr_type  := (others => '0');
39       api_o_tgt_cmd_out : out   seCmd_type      := CMD_WR;
40       api_o_src_reg_out : out   seRegAddr_type  := (others => '0');
41       api_o_src_cmd_out : out   seCmd_type      := CMD_WR;
42       api_o_data_out    : out   seData_type     := (others => '0');
43       api_o_wr_en_out   : out   seFlag_type     := '0';
44       -- INPUT REGISTER PORTS
45       api_i_clk_out     : out   std_logic;
46       api_i_src_slot_in : in    seSlotAddr_type;
47       api_i_src_fpga_in : in    seFpgaAddr_type;
48       api_i_src_reg_in  : in    seRegAddr_type;
49       api_i_src_cmd_in  : in    seCmd_type;
50       api_i_tgt_reg_in  : in    seRegAddr_type;
51       api_i_tgt_cmd_in  : in    seCmd_type;
52       api_i_data_in     : in    seData_type;
53       api_i_empty_in    : in    seFlag_type;
54       api_i_am_empty_in : in    seFlag_type;
55       api_i_rd_en_out   : out   seFlag_type     := '0'
56    );
```

```
57 end entity rivyera_accelerator_main;
58
59 architecture clean_behave of rivyera_accelerator_main is
60    -- Clock connections
61    signal api_i_clk : std_logic;
62    signal api_o_clk : std_logic;
63
64    -- API control signals
65    signal api_i_rd_en : seFlag_type := '0';
66    signal api_o_wr_en : seFlag_type := '0';
67
68    -- Command constants (matching Python)
69    constant CMD_READ  : std_logic_vector(7 downto 0) := x"01";
70    constant CMD_WRITE : std_logic_vector(7 downto 0) := x"02";
71    constant CMD_EXECUTE      : std_logic_vector(7 downto 0) := x"03";
72    constant CMD_STATUS       : std_logic_vector(7 downto 0) := x"04";
73    constant CMD_LOAD_KERNEL  : std_logic_vector(7 downto 0) := x"05";
74
75    constant EXECUTION_STATUS_NOT_COMPLETED : std_logic_vector(63 downto 0) :=
      ↪  x"0000000000000000";
76    constant EXECUTION_STATUS_COMPLETED : std_logic_vector(63 downto 0) :=
      ↪  x"0000000000000001";
77
78    -- Status constants
79    constant STATUS_OK    : std_logic_vector(63 downto 0) := x"0000000000000001";
80    constant STATUS_ERROR : std_logic_vector(63 downto 0) := x"00000000000000FF";
81
82    -- State machine
83    type state_t is (
84       IDLE,           -- Waiting for command
85       READ_CMD,       -- Reading command parameters
86       PROCESS_CMD,    -- Processing the command
87       WAIT_CYCLES,    -- Wait for some cycles
88       WAIT_MEM_OP,
89       SEND_RESPONSE   -- Sending response
90    );
91    signal state : state_t := IDLE;
92
93    -- Generic wait cycle management
94    signal wait_cycles_remaining : integer range 0 to 15 := 0;  -- Countdown
95    signal wait_next_state : state_t := IDLE;  -- What state to go to after waiting
96
97    -- Command processing signals
98    signal cmd_buffer : std_logic_vector(7 downto 0) := (others => '0');
99    signal param1, param2, param3 : std_logic_vector(63 downto 0) := (others => '0');
100   signal param_count : integer := 0;
101   signal params_needed : integer := 0;
```

```
102
103     -- Response signals
104     signal response_data : seData_type := (others => '0');
105     signal response_ready : std_logic := '0';
106
107     -- Kernel load signals
108     signal inst_load_enable : std_logic;
109     signal inst_load_addr : std_logic_vector(15 downto 0) := (others => '0');
110     signal inst_load_data : std_logic_vector(31 downto 0) := (others => '0');
111
112     -- Kernel execution control
113     signal kernel_exec_id     : integer := -1;
114     signal kernel_execute_en  : std_logic;
115     signal kernel_cores_en    : std_logic_vector(NUM_THREADS-1 downto 0);
116     signal kernel_context_rst : std_logic;
117     signal kernel_core_halted : std_logic_vector(NUM_THREADS-1 downto 0) := (others => '0');
118
119     -- Shared memory signals
120     signal shared_mem_addr : std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0) := (others
        ↪  => '0');
121     signal shared_mem_data_in : std_logic_vector(31 downto 0);
122     signal shared_mem_data_out : std_logic_vector(31 downto 0);
123     signal shared_mem_data_out_reg : std_logic_vector(31 downto 0);
124     signal shared_mem_re : std_logic;
125     signal shared_mem_we : std_logic;
126     signal shared_mem_complete : std_logic;
127     signal shared_mem_stall : std_logic;
128
129     -- Current operation context
130     signal current_offset : integer := 0;
131     signal transfer_count : integer := 0;
132     signal transfer_index : integer := 0;
133     signal current_word_half: integer range 0 to 1 := 0;
134     signal current_kernel_load_index : integer := 0;
135
136     -- Array type to hold last 10 sent words
137     type sent_words_array_t is array(0 to 9) of seData_type;
138     signal last_sent_words : sent_words_array_t := (others => (others => '0'));
139     signal sent_words_index : integer range 0 to 9 := 0;
140     signal total_sent_words : integer := 0;
141 begin
142     -- Clock domain assignments
143     api_i_clk <= api_clk_in;
144     api_o_clk <= api_clk_in;
145     api_i_clk_out <= api_i_clk;
146     api_o_clk_out <= api_o_clk;
147
148     -- Route control signals
```

```
149    api_i_rd_en_out <= api_i_rd_en;
150    api_o_wr_en_out <= api_o_wr_en;
151
152    -- LED indicators
153    api_led_out(0) <= '1' when state /= IDLE else '0';
154    api_led_out(1) <= '1' when response_ready = '1' else '0';
155    gen_unused_leds: if NUM_LEDS > 2 generate
156       api_led_out(NUM_LEDS-1 downto 2) <= (others => '0');
157    end generate;
158
159    -- Instantiate multi_core_system
160    multi_core_system: entity work.multi_core_system
161    port map (
162         clk    => api_clk_in,
163         rst    => kernel_context_rst,
164
165         -- Simple control
166         system_enable   => kernel_execute_en,
167         cores_enabled_in => kernel_cores_en,
168
169         -- Instruction loading (broadcast to all cores)
170         inst_load_enable => inst_load_enable,
171         inst_load_addr   => inst_load_addr,
172         inst_load_data   => inst_load_data,
173
174         -- Control outputs
175         core_halted => kernel_core_halted,
176         -- debug_core_pcs    : out std_logic_vector(NUM_CORES*16-1 downto 0);
177
178         -- External memory interface
179         ext_mem_addr     => shared_mem_addr,
180         ext_mem_data_in  => shared_mem_data_in,
181         ext_mem_we       => shared_mem_we,
182         ext_mem_re       => shared_mem_re,
183         ext_mem_data_out => shared_mem_data_out,
184         ext_mem_complete => shared_mem_complete,
185         ext_mem_stall    => shared_mem_stall
186    );
187
188    -- Main state machine process
189    main_proc : process(api_clk_in)
190       variable v_offset : integer;
191       variable v_length : integer;
192       variable v_kernel_exec_id  : integer;
193       variable v_kernel_cores_en : integer;
194       variable v_kernel_exec_completed  : boolean;
195
196       -- Procedure to start waiting for a specified number of cycles
```

```
197      procedure wait_cycles(cycles : integer; next_state : state_t) is
198      begin
199         wait_cycles_remaining <= cycles;
200         wait_next_state <= next_state;
201         state <= WAIT_CYCLES;
202      end procedure;
203
204      procedure wait_mem_op(next_state : state_t) is
205      begin
206         wait_next_state <= next_state;
207         state <= WAIT_MEM_OP;
208      end procedure;
209   begin
210      if rising_edge(api_clk_in) then
211         -- Default assignments
212         api_i_rd_en <= '0';
213         api_o_wr_en <= '0';
214         inst_load_enable <= '0';
215         kernel_context_rst <= '0';
216
217         -- Output addressing (echo back to sender)
218         api_o_tgt_slot_out <= api_i_src_slot_in;
219         api_o_tgt_fpga_out <= api_i_src_fpga_in;
220         api_o_tgt_reg_out  <= api_i_src_reg_in;
221         api_o_tgt_cmd_out  <= api_i_src_cmd_in;
222         api_o_src_reg_out  <= api_i_tgt_reg_in;
223         api_o_src_cmd_out  <= api_i_tgt_cmd_in;
224
225
226         if api_rst_in = '1' then
227            -- Reset everything
228            state <= IDLE;
229            response_ready <= '0';
230         else
231            case state is
232               when IDLE =>
233                  -- Check for incoming data
234                  if api_i_empty_in = '0' then
235                     -- Read the command byte
236                     cmd_buffer <= api_i_data_in(7 downto 0);
237                     api_i_rd_en <= '1';
238                     param_count <= 0;
239
240                     -- For now - always work with a default starting params_needed of 3
241                     params_needed <= 3;
242
243                     state <= READ_CMD;
244                     wait_cycles(2, READ_CMD);
```

```
245                end if;
246             when WAIT_CYCLES =>
247                -- Generic cycle waiting state
248                if wait_cycles_remaining > 0 then
249                   wait_cycles_remaining <= wait_cycles_remaining - 1;
250                else
251                   -- Wait complete, go to next state
252                   state <= wait_next_state;
253                end if;
254             when WAIT_MEM_OP =>
255                shared_mem_we <= '0';
256                shared_mem_re <= '0';
257                if shared_mem_complete = '1' then
258                   shared_mem_data_out_reg <= shared_mem_data_out;
259                   state <= wait_next_state;
260                end if;
261             when READ_CMD =>
262                -- Read command parameters
263                if param_count < params_needed then
264                   if api_i_empty_in = '0' then
265                      if param_count < 3 then
266                         -- Reading initial parameters
267                         case param_count is
268                            when 0 => param1 <= api_i_data_in;
269                            when 1 => param2 <= api_i_data_in;
270                            when 2 => param3 <= api_i_data_in;
271                            when others => null;
272                         end case;
273                         param_count <= param_count + 1;
274                         api_i_rd_en <= '1';
275                         wait_cycles(2, READ_CMD);
276                      else
277                         -- Reading data for write buffer operation
278                         if cmd_buffer = CMD_WRITE then
279                            -- Write data directly to shared memory
280                            -- report "datain on write " & to_hstring(api_i_data_in);
281                         -- report "Initiating write on " & integer'image((current_offset
                               ↪  + transfer_index)*2+current_word_half);
282                            -- report "Writing data " &
                               ↪  to_hstring(api_i_data_in(64-1-32*(1-current_word_half)
                               ↪  downto 32*current_word_half));
283                            shared_mem_data_in <=
                               ↪  api_i_data_in(64-1-32*(1-current_word_half) downto
                               ↪  32*current_word_half);
284                            shared_mem_we <= '1';
285                          shared_mem_addr <= std_logic_vector(to_unsigned((current_offset
                               ↪  + transfer_index)*2+current_word_half,
                               ↪  SHARED_MEM_ADDR_WIDTH));
```

```
286                         if current_word_half = 1 then
287                             api_i_rd_en <= '1';
288                             param_count <= param_count + 1;
289                             transfer_index <= transfer_index + 1;
290                         end if;
291                         current_word_half <= 1-current_word_half;
292                         wait_mem_op(READ_CMD);
293                     end if;
294                 end if;
295             end if;
296         else
297             case cmd_buffer is
298                 when CMD_LOAD_KERNEL =>
299                     v_offset := to_integer(unsigned(param1(31 downto 0)));
300                     v_length := to_integer(unsigned(param2(31 downto 0)));
301                     shared_mem_addr <= std_logic_vector(to_unsigned(v_offset*2,
                    ↪  SHARED_MEM_ADDR_WIDTH));
302                     shared_mem_re <= '1';
303                     current_kernel_load_index <= 0;
304                     wait_mem_op(PROCESS_CMD);
305                 when others =>
306                     -- All parameters read, process command
307                     state <= PROCESS_CMD;
308             end case;
309         end if;
310 
311     when PROCESS_CMD =>
312         -- Process the command
313         case cmd_buffer is
314             when CMD_READ =>
315                 -- Setup for read operation
316                 v_offset := to_integer(unsigned(param1(31 downto 0)));
317                 v_length := to_integer(unsigned(param2(31 downto 0)));
318 
319                 current_offset <= v_offset;
320                 current_word_half <= 0;
321                 transfer_count <= (v_length+7)/8;
322                 transfer_index <= 0;
323 
324                 -- Initiate first read
325                 -- report "Initiating read on " & integer'image(v_offset*2);
326                 shared_mem_addr <= std_logic_vector(to_unsigned(v_offset*2,
                ↪  SHARED_MEM_ADDR_WIDTH));
327                 shared_mem_re <= '1';
328 
329                 -- Send status first
330                 response_data <= STATUS_OK;
```

```
331                     response_ready <= '1';
332
333                     wait_mem_op(SEND_RESPONSE);
334                 when CMD_WRITE =>
335                     -- Setup for write operation
336                     v_offset := to_integer(unsigned(param1(31 downto 0)));
337                     v_length := to_integer(unsigned(param2(31 downto 0)));
338                     if param_count = 3 then
339                         -- Just finished reading parameters, setup for data reading
340                         current_offset <= v_offset;
341                         current_word_half <= 0;
342                         transfer_count <= (v_length+7)/8;
343                         transfer_index <= 0;
344                         -- report "Datain on write start " & to_hstring(api_i_data_in);
345                         -- Continue reading data to write
346                         wait_cycles(1, READ_CMD);
347                         params_needed <= (v_length+7)/8 + params_needed;
348                     else
349                         -- Finished reading all data, send response
350                         response_data <= STATUS_OK;
351                         response_ready <= '1';
352                         state <= SEND_RESPONSE;
353                     end if;
354                 when CMD_LOAD_KERNEL =>
355                   v_offset := to_integer(unsigned(param1(31 downto 0))); -- Address in
                      ↪  8-byte words
356                     v_length := to_integer(unsigned(param2(31 downto 0))); -- Length in
                      ↪  bytes
357                     -- Load instruction
358                     if current_kernel_load_index < v_length / 4 then
359                         inst_load_enable <= '1';
360                         inst_load_data <= shared_mem_data_out_reg;
361                         inst_load_addr <=
                            ↪  std_logic_vector(to_unsigned(current_kernel_load_index,
                            ↪  16));
362                     else
363                         response_data <= STATUS_OK;
364                         response_ready <= '1';
365                         state <= SEND_RESPONSE;
366                     end if;
367                     if current_kernel_load_index + 1 < v_length / 4 then
368                         -- Prepare fetch for next instruction
369                         shared_mem_addr <= std_logic_vector(to_unsigned(v_offset*2 +
                            ↪  current_kernel_load_index + 1, SHARED_MEM_ADDR_WIDTH));
370                         shared_mem_re <= '1';
371                         wait_mem_op(PROCESS_CMD);
372                     end if;
```

```
373                     current_kernel_load_index <= current_kernel_load_index + 1;
374                 when CMD_EXECUTE =>
375                     if kernel_execute_en = '1' and kernel_core_halted = kernel_cores_en
                        ↪  then
376                         -- Reset multicore system, prepare for execution
377                         kernel_execute_en <= '0';
378                         kernel_context_rst <= '1';
379                         wait_cycles(1, PROCESS_CMD);
380                     elsif kernel_execute_en = '1' then
381                         -- Execution still in progress, send failure response
382                         response_data <= STATUS_ERROR;
383                         response_ready <= '1';
384                         state <= SEND_RESPONSE;
385                     else
386                         -- Start execution, send success response
387                         v_kernel_exec_id := to_integer(signed(param1(31 downto 0)));
388                         v_kernel_cores_en := to_integer(signed(param2(31 downto 0)));
389                         kernel_exec_id <= v_kernel_exec_id;
390                         kernel_execute_en <= '1';
391                         for i in 0 to NUM_THREADS-1 loop
392                             if i < v_kernel_cores_en then
393                                 kernel_cores_en(i) <= '1';
394                             else
395                                 kernel_cores_en(i) <= '0';
396                             end if;
397                         end loop;
398                         response_data <= STATUS_OK;
399                         response_ready <= '1';
400                         state <= SEND_RESPONSE;
401                     end if;
402 
403                 when CMD_STATUS =>
404                     v_kernel_exec_id := to_integer(signed(param1(31 downto 0)));
405                     v_kernel_exec_completed := kernel_exec_id = v_kernel_exec_id and
                        ↪  kernel_core_halted = kernel_cores_en;
406                     transfer_index <= 0;
407                     response_data <= STATUS_OK;
408                     response_ready <= '1';
409                     state <= SEND_RESPONSE;
410 
411                 when others =>
412                     -- report "UNKOWN COMMAND PROCESSED";
413                     -- Unknown command
414                     response_data <= STATUS_OK; -- Be permissive for now
415                     response_ready <= '1';
416                     state <= SEND_RESPONSE;
417             end case;
```

```
418
419             when SEND_RESPONSE =>
420                 -- Send response
421                 if api_o_rfd_in = '1' then
422                     api_o_data_out <= response_data;
423                     api_o_wr_en <= response_ready;
424                     response_ready <= '0';
425
426                     if cmd_buffer = CMD_READ and transfer_index < transfer_count then
427                         -- Precondition: shared_mem_data_out_reg contains the data for the
                            ↪  present transfer_index and current_word_half
428                         if transfer_index < transfer_count - current_word_half then
429                             report "Initiating read on " & integer'image((current_offset +
                                ↪  transfer_index + current_word_half)*2 +
                                ↪  1-current_word_half);
430                             shared_mem_addr <= std_logic_vector(to_unsigned((current_offset +
                                ↪  transfer_index + current_word_half)*2 +
                                ↪  1-current_word_half, SHARED_MEM_ADDR_WIDTH));
431                             shared_mem_re <= '1';
432                             wait_mem_op(SEND_RESPONSE);
433                         end if;
434                         report "Sending out response data " &
                            ↪  to_hstring(shared_mem_data_out_reg);
435                         response_data(64-1-32*(1-current_word_half) downto
                            ↪  32*current_word_half) <= shared_mem_data_out_reg;
436                         if current_word_half = 1 then
437                             api_o_data_out <= shared_mem_data_out_reg & response_data(31
                                ↪  downto 0);
438                             api_o_wr_en <= '1';
439                         end if;
440                         transfer_index <= transfer_index+current_word_half;
441                         current_word_half <= 1-current_word_half;
442                     elsif cmd_buffer = CMD_STATUS and transfer_index = 0 then
443                         if v_kernel_exec_completed then
444                             response_data <= EXECUTION_STATUS_COMPLETED;
445                         else
446                             response_data <= EXECUTION_STATUS_NOT_COMPLETED;
447                         end if;
448                         response_ready <= '1';
449                         transfer_index <= 1;
450                     else
451                         -- Done sending
452                         state <= IDLE;
453                     end if;
454                 end if;
455             end case;
456         end if;
```

```
457       end if;
458    end process;
459
460    track_send_proc : process(api_clk_in) begin
461       if rising_edge(api_clk_in) then
462          if api_o_wr_en = '1' then
463             total_sent_words <= total_sent_words + 1;
464             -- if cmd_buffer = CMD_EXECUTE then
465             --    report "SENDING WORD FOR CMD_EXECUTE";
466             -- elsif cmd_buffer = CMD_LOAD_KERNEL then
467             --    report "SENDING WORD FOR CMD_LOAD_KERNEL";
468             -- elsif cmd_buffer = CMD_STATUS then
469             --    report "SENDING WORD FOR CMD_STATUS";
470             -- elsif cmd_buffer = CMD_READ then
471             --    report "SENDING WORD FOR CMD_READ: " & to_hstring(response_data);
472             -- elsif cmd_buffer = CMD_WRITE then
473             --    report "SENDING WORD FOR CMD_READ: " & to_hstring(response_data);
474             -- else
475             --    report "SENDING WORD FOR MISC CMD" & to_hstring(response_data);
476             -- end if;
477             -- Track the sent word in circular buffer
478             -- report "Sending out response word " & to_hstring(response_data);
479             last_sent_words(sent_words_index) <= response_data;
480             if sent_words_index = 9 then
481                sent_words_index <= 0;  -- Wrap around
482             else
483                sent_words_index <= sent_words_index + 1;
484             end if;
485          end if;
486       end if;
487    end process;
488 end architecture clean_behave;
```

## A.2 Compute Core Implementation

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4  use work.types_pkg.all;
5  use work.isa_pkg.all;
6  use work.shared_memory_types.all;
7
8  entity compute_core is
9      generic (
10         NUM_BANKS      : integer := SHARED_MEM_BANKS;      -- Number of memory banks
11         BANK_SIZE      : integer := SHARED_MEM_BANK_SIZE    -- Words per bank
```

```
    );
    port (
        clk             : in  std_logic;
        rst             : in  std_logic;

        -- Control signals
        core_id         : in integer range 0 to NUM_THREADS-1;
        core_enable     : in  std_logic;  -- Enable core execution
        core_halt       : out std_logic;  -- Core has halted

        -- Instruction loading interface
        inst_load_enable: in  std_logic;
        inst_load_addr  : in  std_logic_vector(15 downto 0);
        inst_load_data  : in  instruction_t;

        -- External data memory interface (for shared memory)
        -- Since we're single-threaded, we only use index 0 of the arrays
        ext_mem_addr    : out std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0);
        ext_mem_data_out: out std_logic_vector(31 downto 0);
        ext_mem_we      : out std_logic;
        ext_mem_re      : out std_logic;
        ext_mem_data_in : in  std_logic_vector(31 downto 0);
        ext_mem_complete: in  std_logic;
        ext_mem_stall   : in  std_logic;

        -- Debug outputs (optional)
        debug_pc        : out pc_t;
        debug_inst      : out instruction_t;
        debug_inst_valid: out std_logic;
        debug_mem_inst_valid: out std_logic
    );
end entity compute_core;

architecture rtl of compute_core is
    -- Control signals
    signal core_enable_reg : std_logic;

    -- Pipeline stage interconnect signals
    -- IF -> ID
    signal if_instruction   : instruction_t;
    signal if_inst_valid    : std_logic;
    signal if_thread_id     : thread_id_t;
    signal if_inst_pc       : pc_t;

    -- ID -> EX
    signal id_opcode        : std_logic_vector(5 downto 0);
    signal id_rd_addr       : reg_addr_t := (others => '0');
    signal id_rs1_addr      : reg_addr_t := (others => '0');
```

```
60      signal id_rs2_addr      : reg_addr_t := (others => '0');
61      signal id_rs3_addr      : reg_addr_t := (others => '0');
62      signal id_immediate     : std_logic_vector(15 downto 0);
63      signal id_reg_write_en  : std_logic;
64      signal id_mem_read      : std_logic;
65      signal id_mem_write     : std_logic;
66      signal id_branch        : std_logic;
67      signal id_alu_op        : std_logic_vector(5 downto 0);
68      signal id_alu_src_imm   : std_logic;
69      signal id_thread_id     : thread_id_t;
70      signal id_inst_valid    : std_logic;
71      signal id_inst_pc       : pc_t;
72
73      -- EX -> MEM
74      signal ex_alu_result    : reg_data_t;
75      signal ex_mem_addr      : reg_data_t;
76      signal ex_mem_data      : reg_data_t;
77      signal ex_rd_addr       : reg_addr_t;
78      signal ex_reg_write_en  : std_logic := '0';
79      signal ex_halt_out      : std_logic := '0';
80      signal ex_mem_read      : std_logic := '0';
81      signal ex_mem_write     : std_logic := '0';
82      signal ex_thread_id     : thread_id_t;
83      signal ex_inst_valid    : std_logic := '0';
84
85      -- MEM -> WB
86      signal mem_wb_data      : reg_data_t;
87      signal mem_rd_addr      : reg_addr_t;
88      signal mem_reg_write_en : std_logic;
89      signal mem_thread_id    : thread_id_t;
90      signal mem_inst_valid   : std_logic;
91
92      -- Register file interface
93      signal rf_rs1_data      : reg_data_t;
94      signal rf_rs2_data      : reg_data_t;
95      signal rf_rd_data       : reg_data_t;
96      signal rf_wr_enable     : std_logic;
97      signal rf_wr_addr       : reg_addr_t := (others => '0');
98      signal rf_wr_data       : reg_data_t;
99      signal rf_thread_id     : thread_id_t;
100
101     -- PC Manager interface
102     signal pc_current       : pc_t := (others => '0');
103     signal pc_inc           : std_logic;
104     signal pc_branch_taken  : std_logic;
105     signal pc_branch_target : pc_t;
106
107     -- Forwarding paths
```

```
108     signal fwd_mem_data     : reg_data_t;
109     signal fwd_mem_addr     : reg_addr_t;
110     signal fwd_mem_valid    : std_logic;
111     signal fwd_wb_data      : reg_data_t;
112     signal fwd_wb_addr      : reg_addr_t;
113     signal fwd_wb_valid     : std_logic;
114
115     -- Pipeline control signals
116     signal stall_if         : std_logic;
117     signal stall_id         : std_logic;
118     signal stall_ex         : std_logic;
119     signal stall_mem        : std_logic;
120     signal stall_wb         : std_logic;
121     signal flush_if         : std_logic;
122     signal flush_id         : std_logic;
123     signal flush_ex         : std_logic;
124     signal flush_mem        : std_logic;
125     signal flush_wb         : std_logic;
126
127     -- Hazard detection signals
128     signal load_use_hazard  : std_logic;
129     signal mem_stall_out    : std_logic;
130     signal global_stall     : std_logic;
131
132     -- Shared memory interface adaptation
133     signal mem_addr_array   : addr_array_t;
134     signal mem_data_in_array: data_array_t;
135     signal mem_we_array     : std_logic_vector(NUM_THREADS-1 downto 0);
136     signal mem_re_array     : std_logic_vector(NUM_THREADS-1 downto 0);
137     signal mem_data_out_array: data_array_t;
138     signal mem_complete_array: std_logic_vector(NUM_THREADS-1 downto 0);
139     signal mem_stall_array  : std_logic_vector(NUM_THREADS-1 downto 0);
140
141 begin
142     -- Control signals
143     core_enable_reg <= core_enable and not ex_halt_out;
144
145     -- Debug outputs
146     debug_pc <= pc_current;
147     debug_inst <= if_instruction;
148     debug_inst_valid <= if_inst_valid;
149     debug_mem_inst_valid <= mem_inst_valid;
150
151     -- Hazard detection logic
152     -- Load-use hazard: EX stage needs data that ID stage is loading
153     load_use_hazard <= '1' when (id_inst_valid = '1' and ex_inst_valid = '1' and
        ↪  ex_mem_read = '1' and
154                                 ((id_rs1_addr = ex_rd_addr and unsigned(id_rs1_addr) /= 0) or
```

```
                                (id_rs2_addr = ex_rd_addr and unsigned(id_rs2_addr) /= 0
                                ↪  and id_alu_src_imm = '0')))
                    else '0';

    -- Global stall signal (memory stall affects entire pipeline)
    global_stall <= mem_stall_out;

    -- Pipeline stall logic
    stall_if  <= global_stall or load_use_hazard;
    stall_id  <= global_stall or load_use_hazard;
    stall_ex  <= global_stall;
    stall_mem <= global_stall;
    stall_wb  <= global_stall;

    -- Pipeline flush logic (flush on branch taken)
    flush_if  <= pc_branch_taken;
    flush_id  <= pc_branch_taken;
    flush_ex  <= '0';  -- Don't flush EX and later stages
    flush_mem <= '0';
    flush_wb  <= '0';

    -- PC increment control
    pc_inc <= core_enable_reg and if_inst_valid and not stall_if and not pc_branch_taken;

    -- Instantiate PC Manager
    pc_manager_inst: entity work.pc_manager
    port map (
        clk          => clk,
        rst          => rst,
        thread_id    => core_id,
        pc_out       => pc_current,
        pc_inc       => pc_inc,
        pc_branch    => pc_branch_taken,
        pc_target    => pc_branch_target,
        thread_enable => core_enable_reg
    );

    -- Instantiate Instruction Fetch stage
    if_stage: entity work.instruction_fetch
    port map (
        clk             => clk,
        rst             => rst,
        thread_id       => core_id,
        thread_valid    => core_enable_reg,
        pc_in           => pc_current,
        instruction_out => if_instruction,
        inst_valid      => if_inst_valid,
        inst_pc         => if_inst_pc,
```

```
202         load_enable     => inst_load_enable,
203         load_addr       => inst_load_addr,
204         load_data       => inst_load_data,
205         stall           => stall_if,
206         flush           => flush_if
207     );
208 
209     -- Thread ID passthrough for IF stage
210     if_thread_id <= core_id;
211 
212     -- Instantiate Instruction Decode stage
213     id_stage: entity work.instruction_decoder
214     port map (
215         clk             => clk,
216         rst             => rst,
217         pc_in           => if_inst_pc,
218         instruction_in  => if_instruction,
219         inst_valid_in   => if_inst_valid,
220         thread_id_in    => if_thread_id,
221         opcode          => id_opcode,
222         rd_addr         => id_rd_addr,
223         rs1_addr        => id_rs1_addr,
224         rs2_addr        => id_rs2_addr,
225         rs3_addr        => id_rs3_addr,
226         immediate       => id_immediate,
227         reg_write_en    => id_reg_write_en,
228         mem_read        => id_mem_read,
229         mem_write       => id_mem_write,
230         branch          => id_branch,
231         alu_op          => id_alu_op,
232         alu_src_imm     => id_alu_src_imm,
233         thread_id_out   => id_thread_id,
234         inst_valid_out  => id_inst_valid,
235         inst_pc         => id_inst_pc,
236         stall           => stall_id,
237         flush           => flush_id
238     );
239 
240     -- Instantiate Execute stage
241     ex_stage: entity work.execute_stage
242     port map (
243         clk              => clk,
244         rst              => rst,
245         opcode_in        => id_opcode,
246         rd_addr_in       => id_rd_addr,
247         rs1_addr_in      => id_rs1_addr,
248         rs2_addr_in      => id_rs2_addr,
249         rs3_addr_in      => id_rs3_addr,
```

```
250         immediate_in     => id_immediate,
251         reg_write_en_in  => id_reg_write_en,
252         mem_read_in      => id_mem_read,
253         mem_write_in     => id_mem_write,
254         branch_in        => id_branch,
255         alu_op_in        => id_alu_op,
256         alu_src_imm_in   => id_alu_src_imm,
257         thread_id_in     => id_thread_id,
258         inst_valid_in    => id_inst_valid,
259         rf_rs1_data      => rf_rs1_data,
260         rf_rs2_data      => rf_rs2_data,
261         rf_rd_data       => rf_rd_data,
262         pc_current       => id_inst_pc,
263         pc_branch_taken  => pc_branch_taken,
264         pc_branch_target => pc_branch_target,
265         alu_result_out   => ex_alu_result,
266         mem_addr_out     => ex_mem_addr,
267         mem_data_out     => ex_mem_data,
268         rd_addr_out      => ex_rd_addr,
269         halt_out         => ex_halt_out,
270         reg_write_en_out => ex_reg_write_en,
271         mem_read_out     => ex_mem_read,
272         mem_write_out    => ex_mem_write,
273         thread_id_out    => ex_thread_id,
274         inst_valid_out   => ex_inst_valid,
275         fwd_wb_data      => fwd_wb_data,
276         fwd_wb_addr      => fwd_wb_addr,
277         fwd_wb_valid     => fwd_wb_valid,
278         fwd_mem_data     => fwd_mem_data,
279         fwd_mem_addr     => fwd_mem_addr,
280         fwd_mem_valid    => fwd_mem_valid,
281         stall            => stall_ex,
282         flush            => flush_ex
283     );
284 
285     -- Instantiate Memory stage
286     mem_stage: entity work.memory_stage
287     port map (
288         clk              => clk,
289         rst              => rst,
290         alu_result_in    => ex_alu_result,
291         mem_addr_in      => ex_mem_addr,
292         mem_data_in      => ex_mem_data,
293         rd_addr_in       => ex_rd_addr,
294         reg_write_en_in  => ex_reg_write_en,
295         mem_read_in      => ex_mem_read,
296         mem_write_in     => ex_mem_write,
297         thread_id_in     => ex_thread_id,
```

```
298         inst_valid_in    => ex_inst_valid,
299         wb_data_out      => mem_wb_data,
300         rd_addr_out      => mem_rd_addr,
301         reg_write_en_out => mem_reg_write_en,
302         thread_id_out    => mem_thread_id,
303         inst_valid_out   => mem_inst_valid,
304         fwd_data         => fwd_mem_data,
305         fwd_addr         => fwd_mem_addr,
306         fwd_valid        => fwd_mem_valid,
307         mem_addr_out     => ext_mem_addr,
308         mem_data_out     => ext_mem_data_out,
309         mem_we_out       => ext_mem_we,
310         mem_re_out       => ext_mem_re,
311         mem_read_data_in => ext_mem_data_in,
312         mem_op_complete  => ext_mem_complete,
313         mem_op_stall     => ext_mem_stall,
314         stall            => stall_mem,
315         flush            => flush_mem,
316         stall_out        => mem_stall_out
317     );
318 
319     -- Instantiate Writeback stage
320     wb_stage: entity work.writeback_stage
321     port map (
322         clk              => clk,
323         rst              => rst,
324         wb_data_in       => mem_wb_data,
325         rd_addr_in       => mem_rd_addr,
326         reg_write_en_in  => mem_reg_write_en,
327         thread_id_in     => mem_thread_id,
328         inst_valid_in    => mem_inst_valid,
329         rf_wr_enable     => rf_wr_enable,
330         rf_wr_addr       => rf_wr_addr,
331         rf_wr_data       => rf_wr_data,
332         rf_thread_id     => rf_thread_id,
333         fwd_data         => fwd_wb_data,
334         fwd_addr         => fwd_wb_addr,
335         fwd_valid        => fwd_wb_valid,
336         stall            => stall_wb,
337         flush            => flush_wb
338     );
339 
340     -- Instantiate Register File
341     reg_file: entity work.register_file
342     generic map (
343         NUM_REGS    => NUM_REGS,
344         DATA_WIDTH  => DATA_WIDTH
345     )
```

```
346     port map (
347         clk         => clk,
348         rst         => rst,
349         thread_id   => core_id,
350         rf_rs1_addr => id_rs1_addr,
351         rf_rs2_addr => id_rs2_addr,
352         rf_rd_addr  => id_rd_addr,
353         rf_rs1_data => rf_rs1_data,
354         rf_rs2_data => rf_rs2_data,
355         rf_rd_data  => rf_rd_data,
356         wr_enable   => rf_wr_enable,
357         wr_addr     => rf_wr_addr,
358         wr_data     => rf_wr_data
359     );
360 
361     -- Core halt detection
362     core_halt <= ex_halt_out;
363 
364 end architecture rtl;
```

## A.3 Shared Memory Implementation

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4  use work.types_pkg.all;
5  use work.isa_pkg.all;
6  
7  library UNISIM;
8  use UNISIM.VComponents.all;
9  
10 -- Type definitions for port arrays (must be before entity)
11 package shared_memory_types is
12     constant SHARED_MEM_PORTS   : integer   := NUM_THREADS+1;
13     type addr_array_t is array (0 to SHARED_MEM_PORTS-1) of
       ↪  std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0);  -- ADDR_WIDTH-1 downto 0
14     type data_array_t is array (0 to SHARED_MEM_PORTS-1) of std_logic_vector(31 downto 0);
15 end package shared_memory_types;
16 
17 library IEEE;
18 use IEEE.STD_LOGIC_1164.ALL;
19 use IEEE.NUMERIC_STD.ALL;
20 use work.types_pkg.all;
21 use work.isa_pkg.all;
22 
23 library UNISIM;
```

```
24 use UNISIM.VComponents.all;
25 use work.shared_memory_types.all;
26
27 entity shared_memory is
28     generic (
29         NUM_BANKS     : integer := SHARED_MEM_BANKS;    -- Number of memory banks
30         BANK_SIZE     : integer := SHARED_MEM_BANK_SIZE  -- Words per bank
31     );
32     port (
33         clk : in std_logic;
34         rst : in std_logic;
35
36         -- Port interface arrays (one per thread)
37         -- Inputs
38         addr         : in  addr_array_t;
39         data_in      : in  data_array_t;
40         we           : in  std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
41         re           : in  std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
42
43         -- Outputs
44         data_out     : out data_array_t;
45         op_complete  : out std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
46         op_stall     : out std_logic_vector(SHARED_MEM_PORTS-1 downto 0)
47     );
48 end entity shared_memory;
49
50 architecture rtl of shared_memory is
51     -- Bank selection constants
52     constant BANK_ADDR_BITS : integer := 1;
53     constant OFFSET_BITS    : integer := 16;
54     constant BRAMS_PER_BANK : integer := 120;
55
56     -- BRAM interface types (now we need arrays of arrays)
57     type bram_addr_bank_array_t is array (0 to BRAMS_PER_BANK-1) of std_logic_vector(13
       ↪  downto 0);
58     type bram_addr_array_t is array (0 to NUM_BANKS-1) of bram_addr_bank_array_t;
59     type bram_data_bank_array_t is array (0 to BRAMS_PER_BANK-1) of std_logic_vector(31
       ↪  downto 0);
60     type bram_data_array_t is array (0 to NUM_BANKS-1) of bram_data_bank_array_t;
61     type bram_we_bank_array_t is array (0 to BRAMS_PER_BANK-1) of std_logic_vector(3 downto
       ↪  0);
62     type bram_we_array_t is array (0 to NUM_BANKS-1) of bram_we_bank_array_t;
63
64     -- BRAM signals
65     signal bram_addr_a  : bram_addr_array_t;
66     signal bram_addr_b  : bram_addr_array_t;
67     signal bram_din_b   : bram_data_array_t;
```

```
68      signal bram_dout_a  : bram_data_array_t;
69      signal bram_we_b    : bram_we_array_t;
70      signal bram_en_a    : std_logic_vector(NUM_BANKS-1 downto 0);
71      signal bram_en_b    : std_logic_vector(NUM_BANKS-1 downto 0);
72
73  begin
74      -- Generate BRAM instances
75      gen_banks: for i in 0 to NUM_BANKS-1 generate
76          gen_brams: for j in 0 to BRAMS_PER_BANK-1 generate
77              bank_mem: RAMB16BWER
78              generic map (
79                  DATA_WIDTH_A => 36,
80                  DATA_WIDTH_B => 36,
81                  DOA_REG => 0,
82                  DOB_REG => 0,
83                  INIT_A => X"000000000",
84                  INIT_B => X"000000000",
85                  WRITE_MODE_A => "READ_FIRST",
86                  WRITE_MODE_B => "READ_FIRST",
87                  SIM_DEVICE => "SPARTAN6"
88              )
89              port map (
90                  -- Port A for reads
91                  CLKA  => clk,
92                  ENA   => bram_en_a(i),
93                  WEA   => "0000",
94                  ADDRA => bram_addr_a(i)(j),
95                  DIA   => (others => '0'),
96                  DIPA  => (others => '0'),
97                  DOA   => bram_dout_a(i)(j),
98                  DOPA  => open,
99                  REGCEA => '0',
100                 RSTA  => '0',
101
102                 -- Port B for writes
103                 CLKB  => clk,
104                 ENB   => bram_en_b(i),
105                 WEB   => bram_we_b(i)(j),
106                 ADDRB => bram_addr_b(i)(j),
107                 DIB   => bram_din_b(i)(j),
108                 DIPB  => (others => '0'),
109                 DOB   => open,
110                 DOPB  => open,
111                 REGCEB => '0',
112                 RSTB  => '0'
113             );
114         end generate;
115     end generate;
```

```
116
117     -- Single process for everything
118     main_process: process(clk)
119         -- Port state type
120         type port_state_t is (IDLE, HOOKUP, STATE_ACCESS);
121         type state_array_t is array (0 to SHARED_MEM_PORTS-1) of port_state_t;
122         variable port_states : state_array_t := (others => IDLE);
123
124         -- Bank assignment tracking
125         type bank_assign_array_t is array (0 to SHARED_MEM_PORTS-1) of integer range 0 to
        ↪  NUM_BANKS-1;
126         variable bank_assignments : bank_assign_array_t := (others => 0);
127
128         -- Round-robin counters for each bank
129         type rr_counter_array_t is array (0 to NUM_BANKS-1) of integer range 0 to
        ↪  SHARED_MEM_PORTS-1;
130         variable rr_counters : rr_counter_array_t := (others => 0);
131
132         -- Temporary variables for arbitration
133         type bank_request_array_t is array (0 to NUM_BANKS-1, 0 to SHARED_MEM_PORTS-1) of
        ↪  boolean;
134         variable bank_requests : bank_request_array_t;
135         type bank_grant_array_t is array (0 to NUM_BANKS-1) of integer range -1 to
        ↪  SHARED_MEM_PORTS-1;
136         variable bank_grants : bank_grant_array_t;
137
138         -- Helper variables
139         type mem_request_array_t is array (0 to SHARED_MEM_PORTS-1) of std_logic;
140         type mem_addr_request_array_t is array (0 to SHARED_MEM_PORTS-1) of
        ↪  std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0);
141         variable v_addr_request : addr_array_t := (others => (others => '0'));
142         variable v_we_request : mem_request_array_t;
143         variable v_re_request : mem_request_array_t;
144         variable v_bank : integer range 0 to NUM_BANKS-1;
145         variable v_bank_lock : std_logic_vector(NUM_BANKS-1 downto 0);
146         variable v_offset : std_logic_vector(OFFSET_BITS-1 downto 0);
147         variable v_granted : boolean;
148         variable v_start_port : integer range 0 to SHARED_MEM_PORTS-1;
149         variable v_check_port : integer range 0 to SHARED_MEM_PORTS-1;
150         type op_cycle_array_t is array (0 to SHARED_MEM_PORTS-1) of integer range 0 to 2;
151         variable v_op_cycles : op_cycle_array_t;
152         variable v_bram_select : integer range 0 to BRAMS_PER_BANK-1;
153         variable v_bram_offset : std_logic_vector(8 downto 0); -- 9 bits for 512 words per
        ↪  BRAM
154
155     begin
156         if rising_edge(clk) then
```

```
157             if rst = '1' then
158                 -- Reset all states
159                 port_states := (others => IDLE);
160                 bank_assignments := (others => 0);
161                 rr_counters := (others => 0);
162                 op_complete <= (others => '0');
163                 op_stall <= (others => '0');
164                 data_out <= (others => (others => '0'));
165                 bram_en_a <= (others => '0');
166                 bram_en_b <= (others => '0');
167                 bram_we_b <= (others => (others => "0000"));
168             else
169                 -- Default outputs
170                 op_complete <= (others => '0');
171                 op_stall <= (others => '0');
172 
173                 -- Clear bank requests
174                 bank_requests := (others => (others => false));
175                 bank_grants := (others => -1);
176 
177                 -- Phase 1: Collect requests from ports in IDLE state
178                 for p in 0 to SHARED_MEM_PORTS-1 loop
179                     if port_states(p) = IDLE then
180                         if re(p) = '1' or we(p) = '1' then
181                             -- Extract bank from address
182                             v_bank := to_integer(unsigned(addr(p)(BANK_ADDR_BITS-1 downto
                                ↪  0)));
183                             v_addr_request(p) := addr(p);
184                             v_re_request(p) := re(p);
185                             v_we_request(p) := we(p);
186                             bank_requests(v_bank, p) := true;
187                         end if;
188                     end if;
189                 end loop;
190 
191                 -- Phase 2: Arbitrate bank access (round-robin per bank)
192                 for b in 0 to NUM_BANKS-1 loop
193                     if v_bank_lock(b) /= '1' then
194                         v_granted := false;
195                         v_start_port := rr_counters(b);
196 
197                         -- Check SHARED_MEM_PORTS ports starting from round-robin position
198                         for i in 0 to SHARED_MEM_PORTS-1 loop
199                             v_check_port := (v_start_port + i) mod SHARED_MEM_PORTS;
200 
201                             if bank_requests(b, v_check_port) and not v_granted then
202                                 bank_grants(b) := v_check_port;
203                                 v_granted := true;
```

```
204                             v_bank_lock(b) := '1';
205                             -- Update round-robin counter for next cycle
206                             rr_counters(b) := (v_check_port + 1) mod SHARED_MEM_PORTS;
207                         end if;
208                     end loop;
209                 end if;
210             end loop;
211
212             -- Phase 3: Update port states based on arbitration
213             for p in 0 to SHARED_MEM_PORTS-1 loop
214                 -- Extract bank from lower 3 bits of address
215                 v_bank := to_integer(unsigned(v_addr_request(p)(BANK_ADDR_BITS-1 downto
                    ↪  0)));
216                 -- Extract offset (14 bits)
217                 v_offset := v_addr_request(p)(SHARED_MEM_ADDR_WIDTH-1 downto
                    ↪  BANK_ADDR_BITS);
218                 -- Split offset into BRAM select and BRAM internal offset
219                 v_bram_select := to_integer(unsigned(v_offset(15 downto 9))); -- Upper 7
                    ↪  bits select BRAM
220                 v_bram_offset := v_offset(8 downto 0); -- Lower 9 bits are offset within
                    ↪  BRAM
221                 case port_states(p) is
222                     when IDLE =>
223                         if v_re_request(p) = '1' or v_we_request(p) = '1' then
                            ↪
224                             if bank_grants(v_bank) = p then
225                                 -- This port won arbitration
226                                 port_states(p) := HOOKUP;
227                                 -- report "assigning bank " & integer'image(v_bank) & "
                                    ↪  to port " & integer'image(p) &  " from address " &
                                    ↪  integer'image(to_integer(unsigned(addr(p))));
228                                 bank_assignments(p) := v_bank;
229                             else
230                                 -- This port lost arbitration - stall
231                                 op_stall(p) <= '1';
232                             end if;
233                         end if;
234
235                     when HOOKUP =>
236                         -- Move to STATE_ACCESS state
237                         port_states(p) := STATE_ACCESS;
238
239                         -- Setup BRAM access
240                         v_bank := bank_assignments(p);
241
242                         if v_re_request(p) = '1' then
243                             -- Setup read - only enable the selected BRAM
```

```
244                             bram_addr_a(v_bank)(v_bram_select) <= v_bram_offset & "00000";
245                                 bram_en_a(v_bank) <= '1';
246                                 v_op_cycles(p) := 2;
247                                 -- report "setup read";
248                             elsif v_we_request(p) = '1' then
249                                 -- Setup write
250                             bram_addr_b(v_bank)(v_bram_select) <= v_bram_offset & "00000";
251                                 bram_din_b(v_bank)(v_bram_select) <= data_in(p);
252                                 bram_we_b(v_bank)(v_bram_select) <= "1111";
253                                 bram_en_b(v_bank) <= '1';
254                                 v_op_cycles(p) := 1;
255                             end if;
256
257                         when STATE_ACCESS =>
258                             -- Complete operation
259                             v_bank := bank_assignments(p);
260
261                             if (v_op_cycles(p) < 2) then
262                                 if v_re_request(p) = '1' then
263                                     data_out(p) <= bram_dout_a(v_bank)(v_bram_select);
264                                 end if;
265                                 bram_en_a(v_bank) <= '0';
266                                 bram_en_b(v_bank) <= '0';
267                                 bram_we_b(v_bank)(0) <= "0000"; -- This line seems to be a
                                    ↪  leftover from the old logic, should be v_bram_select
268                                 -- report "completing op";
269                                 op_complete(p) <= '1';
270                                 port_states(p) := IDLE;
271                                 v_re_request(p) := '0';
272                                 v_we_request(p) := '0';
273                                 v_bank_lock(v_bank) := '0';
274                             end if;
275                             v_op_cycles(p) := v_op_cycles(p) - 1;
276                         end case;
277                 end loop;
278             end if;
279         end if;
280     end process;
281
282 end architecture rtl;
```

## A.4 Multi-Core System Implementation

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
```

```
use work.types_pkg.all;
use work.isa_pkg.all;
use work.shared_memory_types.all;

entity multi_core_system is
    generic (
        NUM_CORES     : integer := NUM_THREADS;      -- Start with 4 cores
        NUM_BANKS     : integer := SHARED_MEM_BANKS; -- Memory banks
        BANK_SIZE     : integer := 512     -- Words per bank
    );
    port (
        clk : in std_logic;
        rst : in std_logic;

        -- Simple control
        system_enable : in std_logic;

        cores_enabled_in : in std_logic_vector(NUM_CORES - 1 downto 0);

        -- Instruction loading (broadcast to all cores)
        inst_load_enable : in std_logic;
        inst_load_addr   : in std_logic_vector(15 downto 0);
        inst_load_data   : in instruction_t;

        -- Control outputs
        core_halted : out std_logic_vector(NUM_CORES-1 downto 0);

        -- Debug outputs
        debug_core_pcs    : out std_logic_vector(NUM_CORES*16-1 downto 0);

        -- External memory interface
        ext_mem_addr     : in  std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0);
        ext_mem_data_in  : in  std_logic_vector(31 downto 0);
        ext_mem_we       : in  std_logic;
        ext_mem_re       : in  std_logic;
        ext_mem_data_out : out std_logic_vector(31 downto 0);
        ext_mem_complete : out std_logic;
        ext_mem_stall    : out std_logic
    );
end entity multi_core_system;

architecture rtl of multi_core_system is
    -- Core control signals
    signal core_enables : std_logic_vector(NUM_CORES-1 downto 0);
    signal core_halts   : std_logic_vector(NUM_CORES-1 downto 0);

    -- Memory interface arrays (map cores to shared memory ports)
    constant EXT_MEM_PORT : integer := SHARED_MEM_PORTS-1;
```

```
52      signal mem_addr     : addr_array_t := (others => (others => '0'));
53      signal mem_data_out : data_array_t;
54      signal mem_we       : std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
55      signal mem_re       : std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
56      signal mem_data_in  : data_array_t;
57      signal mem_complete : std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
58      signal mem_stall    : std_logic_vector(SHARED_MEM_PORTS-1 downto 0);
59
60      -- Debug signals
61      type pc_array_type is array (0 to NUM_CORES-1) of pc_t;
62      signal debug_pcs : pc_array_type;
63
64  begin
65      -- All cores enabled when system is enabled
66      core_enables <= cores_enabled_in when system_enable='1' else (others => '0');
67
68      -- Debug outputs
69      core_halted <= core_halts;
70
71      -- Pack debug PCs into single vector
72      gen_debug_pcs: for i in 0 to NUM_CORES-1 generate
73          debug_core_pcs((i+1)*16-1 downto i*16) <= debug_pcs(i);
74      end generate;
75
76      -- Generate cores
77      gen_cores: for i in 0 to NUM_CORES-1 generate
78          core_inst: entity work.compute_core
79          generic map (
80              NUM_BANKS     => NUM_BANKS,
81              BANK_SIZE     => BANK_SIZE
82          )
83          port map (
84              clk             => clk,
85              rst             => rst,
86              core_enable     => core_enables(i),
87              core_halt       => core_halts(i),
88              inst_load_enable => inst_load_enable,  -- Broadcast to all cores
89              inst_load_addr  => inst_load_addr,
90              inst_load_data  => inst_load_data,
91              -- Connect to shared memory using core ID as port index
92              ext_mem_addr    => mem_addr(i),
93              ext_mem_data_out => mem_data_out(i),
94              ext_mem_we      => mem_we(i),
95              ext_mem_re      => mem_re(i),
96              ext_mem_data_in  => mem_data_in(i),
97              ext_mem_complete => mem_complete(i),
98              ext_mem_stall   => mem_stall(i),
99              debug_pc        => debug_pcs(i),
```

```
            core_id       => i
        );
    end generate;

    -- Connect external memory interface to shared_memory
    mem_addr(EXT_MEM_PORT)     <= ext_mem_addr;
    mem_data_out(EXT_MEM_PORT) <= ext_mem_data_in;
    mem_we(EXT_MEM_PORT)       <= ext_mem_we;
    mem_re(EXT_MEM_PORT)       <= ext_mem_re;
    ext_mem_data_out           <= mem_data_in(EXT_MEM_PORT);
    ext_mem_complete           <= mem_complete(EXT_MEM_PORT);
    ext_mem_stall              <= mem_stall(EXT_MEM_PORT);

    -- Clear unused memory ports
    clear_unused: for i in NUM_CORES+1 to EXT_MEM_PORT-1 generate
        mem_addr(i) <= (others => '0');
        mem_data_out(i) <= (others => '0');
        mem_we(i) <= '0';
        mem_re(i) <= '0';
    end generate;

    -- Instantiate shared memory
    shared_mem: entity work.shared_memory
    generic map (
        NUM_BANKS => NUM_BANKS,
        BANK_SIZE => BANK_SIZE
    )
    port map (
        clk         => clk,
        rst         => rst,
        addr        => mem_addr,
        data_in     => mem_data_out,
        we          => mem_we,
        re          => mem_re,
        data_out    => mem_data_in,
        op_complete => mem_complete,
        op_stall    => mem_stall
    );

end architecture rtl;
```

## A.5 Register File

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
```

```
use work.types_pkg.all;

entity register_file is
    generic (
        NUM_REGS    : integer := 32;  -- Registers per thread
        DATA_WIDTH  : integer := 32   -- Start with 32-bit
    );
    port (
        clk         : in  std_logic;
        rst         : in  std_logic;

        -- Thread selection
        thread_id   : in  thread_id_t;

        -- Read ports
        rf_rs1_addr    : in  reg_addr_t;
        rf_rs2_addr    : in  reg_addr_t;
        rf_rd_addr     : in  reg_addr_t;
        rf_rs1_data    : out reg_data_t;
        rf_rs2_data    : out reg_data_t;
        rf_rd_data     : out reg_data_t;

        -- Write port
        wr_enable   : in  std_logic;
        wr_addr     : in  reg_addr_t;
        wr_data     : in  reg_data_t
    );
end entity register_file;

architecture rtl of register_file is
    -- Register array: [thread][register]
    type reg_array_t is array (0 to NUM_REGS-1) of reg_data_t;
    signal thread_reg: reg_data_t := (others => '0');
    signal registers : reg_array_t := (others => (others => '0'));

    -- Special register r0 is always 0 (like MIPS)
    constant REG_ZERO : integer := 0;
    -- Special register r31 is always the thread_id
    constant REG_THREAD : integer := 31;

begin
    -- R31 is always equal to thread_id
    thread_reg <= std_logic_vector(to_unsigned(thread_id, 32));

    -- Asynchronous read
    read_process: process(rf_rs1_addr, rf_rs2_addr, rf_rd_addr)
    begin
        rf_rs1_data <= registers(to_integer(unsigned(rf_rs1_addr)));
```

```
52          rf_rs2_data <= registers(to_integer(unsigned(rf_rs2_addr)));
53          rf_rd_data <= registers(to_integer(unsigned(rf_rd_addr)));
54          if to_integer(unsigned(rf_rs1_addr)) = REG_THREAD then
55              rf_rs1_data <= thread_reg;
56          end if;
57          if to_integer(unsigned(rf_rs2_addr)) = REG_THREAD then
58              rf_rs2_data <= thread_reg;
59          end if;
60          if to_integer(unsigned(rf_rd_addr)) = REG_THREAD then
61              rf_rd_data <= thread_reg;
62          end if;
63      end process;
64
65      -- Synchronous write
66      write_process: process(clk)
67      begin
68          if rising_edge(clk) then
69              if rst = '1' then
70                  -- Reset all registers except r0
71                  for r in 1 to NUM_REGS-1 loop
72                      registers(r) <= (others => '0');
73                  end loop;
74              elsif wr_enable = '1' and unsigned(wr_addr) /= REG_ZERO then
75                  -- Write to register (except r0)
76                  registers(to_integer(unsigned(wr_addr))) <= wr_data;
77              end if;
78          end if;
79      end process;
80
81  end architecture rtl;
```

## A.6 Instruction Fetch

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3   use IEEE.NUMERIC_STD.ALL;
4   use work.types_pkg.all;
5
6   library UNISIM;
7   use UNISIM.VComponents.all;
8
9   entity instruction_fetch is
10      port (
11          clk             : in  std_logic;
12          rst             : in  std_logic;
13
```

```
14          -- From thread scheduler
15          thread_id       : in  thread_id_t;
16          thread_valid    : in  std_logic;
17
18          -- From PC manager
19          pc_in           : in  pc_t;
20
21          -- Instruction output
22          instruction_out : out instruction_t;
23          inst_valid      : out std_logic;
24          inst_pc         : out pc_t;
25
26          -- Memory loading interface (for kernel loading)
27          load_enable     : in  std_logic;
28          load_addr       : in  std_logic_vector(15 downto 0);
29          load_data       : in  instruction_t;
30
31          -- Pipeline control
32          stall           : in  std_logic;
33          flush           : in  std_logic
34      );
35  end entity instruction_fetch;
36
37  architecture rtl of instruction_fetch is
38      -- Calculate address widths
39      constant TOTAL_ADDR_WIDTH : integer := 13;
40      constant BRAM_ADDR_WIDTH  : integer := 9;
41      constant NUM_BRAMS        : integer := 16;
42
43      -- BRAM signals (one set per BRAM)
44      type bram_addr_array_t is array (0 to NUM_BRAMS-1) of std_logic_vector(13 downto 0);
45      type bram_data_array_t is array (0 to NUM_BRAMS-1) of std_logic_vector(31 downto 0);
46      type bram_we_array_t is array (0 to NUM_BRAMS-1) of std_logic_vector(3 downto 0);
47
48      signal bram_addr_a : bram_addr_array_t;
49      signal bram_addr_b : bram_addr_array_t;
50      signal bram_dout   : bram_data_array_t;
51      signal bram_we     : bram_we_array_t;
52      signal bram_en_a   : std_logic_vector(NUM_BRAMS-1 downto 0);
53      signal bram_en_b   : std_logic_vector(NUM_BRAMS-1 downto 0);
54
55      -- Pipeline registers
56      signal instruction_reg : instruction_t;
57      signal valid_reg       : std_logic;
58      signal thread_id_reg   : thread_id_t;
59
60      -- Address calculation
```

```
61      signal fetch_addr      : std_logic_vector(TOTAL_ADDR_WIDTH-1 downto 0) := (others =>
        ↪  '0');
62      signal bram_select     : integer range 0 to NUM_BRAMS-1;
63      signal bram_local_addr : std_logic_vector(BRAM_ADDR_WIDTH-1 downto 0);
64
65      -- Load address decoding
66      signal load_bram_select     : integer range 0 to NUM_BRAMS-1;
67      signal load_bram_local_addr : std_logic_vector(BRAM_ADDR_WIDTH-1 downto 0);
68
69      -- Mux output
70      signal selected_instruction : std_logic_vector(31 downto 0);
71      signal bram_select_reg      : integer range 0 to NUM_BRAMS-1;
72
73  begin
74      -- TODO check if this is fine that we currently can't really store all of the
        ↪  instructions that can be adressed
75      -- with pc_in with our 16 KB of BRAM
76      fetch_addr <= pc_in(TOTAL_ADDR_WIDTH-1 downto 0) when thread_valid = '1' else (others
        ↪  => '0');
77
78      -- Decode which BRAM to access
79      bram_select <= to_integer(unsigned(fetch_addr(TOTAL_ADDR_WIDTH-1 downto
        ↪  BRAM_ADDR_WIDTH)));
80      bram_local_addr <= fetch_addr(BRAM_ADDR_WIDTH-1 downto 0);
81
82      -- Load address decoding
83      load_bram_select <= to_integer(unsigned(load_addr(TOTAL_ADDR_WIDTH-1 downto
        ↪  BRAM_ADDR_WIDTH)));
84      load_bram_local_addr <= load_addr(BRAM_ADDR_WIDTH-1 downto 0);
85
86      -- Generate BRAM instances
87      gen_brams: for i in 0 to NUM_BRAMS-1 generate
88          -- Enable signals for each BRAM
89          bram_en_a(i) <= '1' when (bram_select = i and thread_valid = '1') else '0';
90          bram_en_b(i) <= '1' when (load_bram_select = i and load_enable = '1') else '0';
91
92          -- Write enable only during load and when this BRAM is selected
93          bram_we(i) <= "1111" when (load_bram_select = i and load_enable = '1') else "0000";
94
95          -- Extend addresses to 14 bits for BRAM (pad with zeros)
96          bram_addr_a(i) <= bram_local_addr & "00000";
97          bram_addr_b(i) <= load_bram_local_addr & "00000";
98
99          -- Instruction memory using Spartan-6 BRAM
100         inst_mem: RAMB16BWER
101         generic map (
102             DATA_WIDTH_A => 36,
```

```
103             DATA_WIDTH_B => 36,
104             DOA_REG => 0,
105             DOB_REG => 0,
106             INIT_A => X"000000000",
107             INIT_B => X"000000000",
108             WRITE_MODE_A => "READ_FIRST",
109             WRITE_MODE_B => "READ_FIRST",
110             SIM_DEVICE => "SPARTAN6"
111         )
112         port map (
113             -- Port A for reading
114             CLKA  => clk,
115             ENA   => bram_en_a(i),
116             WEA   => "0000",  -- Read only
117             ADDRA => bram_addr_a(i),
118             DIA   => (others => '0'),
119             DIPA  => (others => '0'),
120             DOA   => bram_dout(i),
121             DOPA  => open,
122             REGCEA => '0',
123             RSTA  => '0',
124 
125             -- Port B for loading
126             CLKB  => clk,
127             ENB   => bram_en_b(i),
128             WEB   => bram_we(i),
129             ADDRB => bram_addr_b(i),
130             DIB   => load_data,
131             DIPB  => (others => '0'),
132             DOB   => open,
133             DOPB  => open,
134             REGCEB => '0',
135             RSTB  => '0'
136         );
137     end generate;
138 
139     -- Multiplexer to select the output from the correct BRAM
140     -- We need to register the BRAM select to align with the BRAM output
141     mux_process: process(clk)
142     begin
143         if rising_edge(clk) then
144             if rst = '1' then
145                 bram_select_reg <= 0;
146             elsif stall = '0' then
147                 bram_select_reg <= bram_select;
148             end if;
149         end if;
150     end process;
```

```
151
152     -- Select the output from the correct BRAM
153     selected_instruction <= bram_dout(bram_select_reg);
154
155     -- Pipeline register process
156     pipeline_reg: process(clk)
157     begin
158         if rising_edge(clk) then
159             if rst = '1' then
160                 valid_reg <= '0';
161                 thread_id_reg <= 0;
162                 inst_pc <= (others => '0');
163             elsif flush = '1' then
164                 -- Flush pipeline
165                 valid_reg <= '0';
166             elsif stall = '0' then
167                 -- Normal operation
168                 valid_reg <= thread_valid;
169                 inst_pc <= pc_in;
170                 thread_id_reg <= thread_id;
171             end if;
172             -- If stalled, hold current values
173         end if;
174     end process;
175
176     -- Output assignments
177     instruction_reg <= selected_instruction;
178     instruction_out <= instruction_reg;
179     inst_valid <= valid_reg;
180
181 end architecture rtl;
```

## A.7 Instruction Decoder

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4  use work.types_pkg.all;
5  use work.isa_pkg.all;
6
7  entity instruction_decoder is
8      port (
9          clk             : in  std_logic;
10         rst             : in  std_logic;
11
12         -- From fetch stage
```

```
        pc_in           : in  pc_t;
        instruction_in  : in  instruction_t;
        inst_valid_in   : in  std_logic;
        thread_id_in    : in  thread_id_t;

        -- Decoded outputs
        opcode          : out std_logic_vector(5 downto 0);
        rd_addr         : out reg_addr_t;
        rs1_addr        : out reg_addr_t;
        rs2_addr        : out reg_addr_t;
        rs3_addr        : out reg_addr_t;  -- For MULACC
        immediate       : out std_logic_vector(15 downto 0);

        -- Control signals
        reg_write_en    : out std_logic;
        mem_read        : out std_logic;
        mem_write       : out std_logic;
        branch          : out std_logic;
        alu_op          : out std_logic_vector(5 downto 0);
        alu_src_imm     : out std_logic;  -- Use immediate instead of rs2

        -- Thread info passthrough
        thread_id_out   : out thread_id_t;
        inst_valid_out  : out std_logic;
        inst_pc         : out pc_t;

        -- Pipeline control
        stall           : in  std_logic;
        flush           : in  std_logic
    );
end entity instruction_decoder;

architecture rtl of instruction_decoder is
    -- Instruction fields
    signal opcode_field : std_logic_vector(5 downto 0);
    signal rd_field     : std_logic_vector(4 downto 0);
    signal rs1_field    : std_logic_vector(4 downto 0);
    signal rs2_field    : std_logic_vector(4 downto 0);
    signal rs3_field    : std_logic_vector(4 downto 0);
    signal imm_field    : std_logic_vector(15 downto 0);

    -- Pipeline registers
    signal opcode_reg       : std_logic_vector(5 downto 0);
    signal rd_reg           : reg_addr_t := (others => '0');
    signal rs1_reg          : reg_addr_t := (others => '0');
    signal rs2_reg          : reg_addr_t := (others => '0');
    signal rs3_reg          : reg_addr_t := (others => '0');
    signal immediate_reg    : std_logic_vector(15 downto 0);
```

```
61      signal reg_write_en_reg : std_logic;
62      signal mem_read_reg     : std_logic;
63      signal mem_write_reg    : std_logic;
64      signal branch_reg       : std_logic;
65      signal alu_op_reg       : std_logic_vector(5 downto 0);
66      signal alu_src_imm_reg  : std_logic;
67      signal thread_id_reg    : thread_id_t;
68      signal inst_valid_reg   : std_logic;
69
70  begin
71      -- Extract instruction fields based on format
72      -- R-type: [31:26] opcode, [25:21] rd, [20:16] rs1, [15:11] rs2, [10:0] unused
73      -- I-type: [31:26] opcode, [25:21] rd, [20:16] rs1, [15:0] immediate
74      opcode_field <= instruction_in(31 downto 26);
75      rd_field     <= instruction_in(25 downto 21);
76      rs1_field    <= instruction_in(20 downto 16);
77      rs2_field    <= instruction_in(15 downto 11);
78      rs3_field    <= "00000";  -- Not used in this ISA version
79      imm_field    <= instruction_in(15 downto 0);
80
81      -- Combinational decode logic
82      decode_proc: process(clk)
83          variable v_reg_write  : std_logic;
84          variable v_mem_read   : std_logic;
85          variable v_mem_write  : std_logic;
86          variable v_branch     : std_logic;
87          variable v_alu_op     : std_logic_vector(5 downto 0);
88          variable v_alu_src    : std_logic;
89      begin
90          if rising_edge(clk) then
91              -- Default values
92              v_reg_write := '0';
93              v_mem_read  := '0';
94              v_mem_write := '0';
95              v_branch    := '0';
96              v_alu_op    := ALU_PASS_A;
97              v_alu_src   := '0';
98
99              if inst_valid_in = '1' then
100                 case opcode_field is
101                     -- Arithmetic R-type
102                     when OP_ADD =>
103                         v_reg_write := '1';
104                         v_alu_op := ALU_ADD;
105
106                     when OP_SUB =>
107                         v_reg_write := '1';
108                         v_alu_op := ALU_SUB;
```

```
109
110                 when OP_MUL =>
111                     v_reg_write := '1';
112                     v_alu_op := ALU_MUL;
113
114                 when OP_DIV =>
115                     v_reg_write := '1';
116                     v_alu_op := ALU_DIV;
117
118                 when OP_MOD =>
119                     v_reg_write := '1';
120                     v_alu_op := ALU_MOD;
121
122                 when OP_AND =>
123                     v_reg_write := '1';
124                     v_alu_op := ALU_AND;
125
126                 when OP_OR =>
127                     v_reg_write := '1';
128                     v_alu_op := ALU_OR;
129
130                 when OP_XOR =>
131                     v_reg_write := '1';
132                     v_alu_op := ALU_XOR;
133
134                 when OP_SHL =>
135                     v_reg_write := '1';
136                     v_alu_op := ALU_SHL;
137
138                 when OP_SHR =>
139                     v_reg_write := '1';
140                     v_alu_op := ALU_SHR;
141
142                 when OP_CMPLT =>
143                     v_reg_write := '1';
144                     v_alu_op := ALU_CMPLT;
145
146                 when OP_CMPNE =>
147                     v_reg_write := '1';
148                     v_alu_op := ALU_CMPNE;
149
150                 when OP_MAX =>
151                     v_reg_write := '1';
152                     v_alu_op := ALU_MAX;
153
154                 when OP_NEG =>
155                     v_reg_write := '1';
156                     v_alu_op := ALU_NEG;
```

```
157
158                     -- Floating point operations
159                     when OP_FADD =>
160                         v_reg_write := '1';
161                         v_alu_op := ALU_FADD;
162
163                     when OP_FSUB =>
164                         v_reg_write := '1';
165                         v_alu_op := ALU_FSUB;
166
167                     when OP_FMUL =>
168                         v_reg_write := '1';
169                         v_alu_op := ALU_FMUL;
170
171                     when OP_FDIV =>
172                         v_reg_write := '1';
173                         v_alu_op := ALU_FDIV;
174
175                     when OP_FSQRT =>
176                         v_reg_write := '1';
177                         v_alu_op := ALU_FSQRT;
178
179                     when OP_FRECIP =>
180                         v_reg_write := '1';
181                         v_alu_op := ALU_FRECIP;
182
183                     when OP_FEXP2 =>
184                         v_reg_write := '1';
185                         v_alu_op := ALU_FEXP2;
186
187                     when OP_FLOG2 =>
188                         v_reg_write := '1';
189                         v_alu_op := ALU_FLOG2;
190
191                     when OP_FMAX =>
192                         v_reg_write := '1';
193                         v_alu_op := ALU_FMAX;
194
195                     when OP_FNEG =>
196                         v_reg_write := '1';
197                         v_alu_op := ALU_FNEG;
198
199                     when OP_FNE =>
200                         v_reg_write := '1';
201                         v_alu_op := ALU_FNE;
202
203                     when OP_FLT =>
204                         v_reg_write := '1';
```

```
205                     v_alu_op := ALU_FLT;
206
207                 when OP_FTOI =>
208                     v_reg_write := '1';
209                     v_alu_op := ALU_FTOI;
210
211                 when OP_FTOUI =>
212                     v_reg_write := '1';
213                     v_alu_op := ALU_FTOUI;
214
215                 when OP_ITOF =>
216                     v_reg_write := '1';
217                     v_alu_op := ALU_ITOF;
218
219                 when OP_UITOF =>
220                     v_reg_write := '1';
221                     v_alu_op := ALU_UITOF;
222
223                 -- Move operations
224                 when OP_MOV =>
225                     v_reg_write := '1';
226                     v_alu_op := ALU_PASS_A;
227
228                 when OP_LOAD_IMM =>
229                     v_reg_write := '1';
230                     v_alu_src := '1';
231                     v_alu_op := ALU_PASS_B;
232
233                 -- Memory operations
234                 when OP_LOAD =>
235                     v_reg_write := '1';
236                     v_mem_read := '1';
237                     v_alu_src := '1';
238                     v_alu_op := ALU_ADD;  -- Address calculation
239
240                 when OP_STORE =>
241                     v_mem_write := '1';
242                     v_alu_src := '1';
243                     v_alu_op := ALU_ADD;  -- Address calculation
244
245                 -- Branch operations
246                 when OP_JMP =>
247                     v_branch := '1';
248
249                 when OP_JZ | OP_JNZ | OP_JLT | OP_JGE =>
250                     v_branch := '1';
251                     v_alu_op := ALU_CMPLT;  -- Use for condition check
252
```

```
253                     -- Special operations
254                     when OP_BARRIER =>
255                         null;  -- Barrier operation - no register write, handled by pipeline
                            ↪  control
256
257                     when OP_HALT =>
258                         null;  -- Halt operation - no register write, handled by pipeline
                            ↪  control
259
260                     when OP_NOP =>
261                         null;  -- No operation
262
263                     when others =>
264                         null;  -- Unknown opcode
265                 end case;
266             end if;
267
268             -- Assign to pipeline registers input
269             reg_write_en_reg <= v_reg_write;
270             mem_read_reg     <= v_mem_read;
271             mem_write_reg    <= v_mem_write;
272             branch_reg       <= v_branch;
273             alu_op_reg       <= v_alu_op;
274             alu_src_imm_reg  <= v_alu_src;
275         end if;
276     end process;
277
278     -- Pipeline register
279     pipeline_reg: process(clk)
280     begin
281         if rising_edge(clk) then
282             if rst = '1' or flush = '1' then
283                 opcode_reg      <= (others => '0');
284                 rd_reg          <= (others => '0');
285                 rs1_reg         <= (others => '0');
286                 rs2_reg         <= (others => '0');
287                 rs3_reg         <= (others => '0');
288                 immediate_reg   <= (others => '0');
289                 thread_id_reg   <= 0;
290                 inst_valid_reg  <= '0';
291                 inst_pc         <= (others => '0');
292             elsif stall = '0' then
293                 opcode_reg      <= opcode_field;
294                 rd_reg          <= rd_field;
295                 rs1_reg         <= rs1_field;
296                 rs2_reg         <= rs2_field;
297                 rs3_reg         <= rs3_field;
```

```
298                 immediate_reg   <= imm_field;
299                 thread_id_reg   <= thread_id_in;
300                 inst_valid_reg  <= inst_valid_in;
301                 inst_pc         <= pc_in;
302             end if;
303         end if;
304     end process;
305 
306     -- Output assignments
307     opcode         <= opcode_reg;
308     rd_addr        <= rd_reg;
309     rs1_addr       <= rs1_reg;
310     rs2_addr       <= rs2_reg;
311     rs3_addr       <= rs3_reg;
312     immediate      <= immediate_reg;
313     reg_write_en   <= reg_write_en_reg and inst_valid_reg;
314     mem_read       <= mem_read_reg and inst_valid_reg;
315     mem_write      <= mem_write_reg and inst_valid_reg;
316     branch         <= branch_reg and inst_valid_reg;
317     alu_op         <= alu_op_reg;
318     alu_src_imm    <= alu_src_imm_reg;
319     thread_id_out  <= thread_id_reg;
320     inst_valid_out <= inst_valid_reg;
321 
322 end architecture rtl;
```

## A.8 Execution Stage

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4  use work.types_pkg.all;
5  use work.isa_pkg.all;
6 
7  entity execute_stage is
8      port (
9          clk             : in  std_logic;
10         rst             : in  std_logic;
11 
12         -- From decode stage
13         opcode_in       : in  std_logic_vector(5 downto 0);
14         rd_addr_in      : in  reg_addr_t;
15         rs1_addr_in     : in  reg_addr_t;
16         rs2_addr_in     : in  reg_addr_t;
17         rs3_addr_in     : in  reg_addr_t;
18         immediate_in    : in  std_logic_vector(15 downto 0);
```

```
19
20          -- Control signals from decode
21          reg_write_en_in : in  std_logic;
22          mem_read_in     : in  std_logic;
23          mem_write_in    : in  std_logic;
24          branch_in       : in  std_logic;
25          alu_op_in       : in  std_logic_vector(5 downto 0);
26          alu_src_imm_in  : in  std_logic;
27
28          -- Thread info
29          thread_id_in    : in  thread_id_t;
30          inst_valid_in   : in  std_logic;
31
32          -- Register file interface
33          rf_rs1_data     : in  reg_data_t;
34          rf_rs2_data     : in  reg_data_t;
35          rf_rd_data      : in  reg_data_t;
36
37          -- PC interface
38          pc_current      : in  pc_t;
39          pc_branch_taken : out std_logic;
40          pc_branch_target: out pc_t;
41
42          -- Outputs to memory stage
43          alu_result_out  : out reg_data_t;
44          mem_addr_out    : out reg_data_t;
45          mem_data_out    : out reg_data_t;
46          rd_addr_out     : out reg_addr_t;
47          halt_out        : out std_logic;
48
49          -- Control signals passthrough
50          reg_write_en_out: out std_logic;
51          mem_read_out    : out std_logic;
52          mem_write_out   : out std_logic;
53
54          -- Thread info passthrough
55          thread_id_out   : out thread_id_t;
56          inst_valid_out  : out std_logic;
57
58          -- Forwarding inputs (from WB and MEM stages)
59          fwd_wb_data     : in  reg_data_t;
60          fwd_wb_addr     : in  reg_addr_t;
61          fwd_wb_valid    : in  std_logic;
62          fwd_mem_data    : in  reg_data_t;
63          fwd_mem_addr    : in  reg_addr_t;
64          fwd_mem_valid   : in  std_logic;
65
66          -- Pipeline control
```

```
67          stall           : in  std_logic;
68          flush           : in  std_logic
69      );
70  end entity execute_stage;
71
72  architecture rtl of execute_stage is
73      -- ALU instance signals
74      signal alu_a        : reg_data_t;
75      signal alu_b        : reg_data_t;
76      signal alu_c        : reg_data_t;
77      signal alu_result   : reg_data_t;
78      signal alu_zero     : std_logic;
79      signal alu_negative : std_logic;
80      signal alu_busy     : std_logic;
81      signal alu_valid    : std_logic;
82
83      -- Forwarded operand values
84      signal operand1     : reg_data_t;
85      signal operand2     : reg_data_t;
86
87      -- Pipeline registers
88      signal halt_reg         : std_logic := '0';
89      signal alu_result_reg   : reg_data_t;
90      signal mem_addr_reg     : reg_data_t;
91      signal mem_data_reg     : reg_data_t;
92      signal rd_addr_reg      : reg_addr_t;
93      signal reg_write_en_reg : std_logic;
94      signal mem_read_reg     : std_logic;
95      signal mem_write_reg    : std_logic;
96      signal thread_id_reg    : thread_id_t;
97      signal inst_valid_reg   : std_logic;
98
99      -- Branch logic signals
100     signal branch_condition : std_logic;
101     signal branch_target    : pc_t;
102
103 begin
104     -- Register file read address assignment
105     operand1 <= rf_rs1_data when get_inst_fmt(opcode_in) = FMT_R_TYPE else rf_rd_data;
106     operand2 <= rf_rs2_data when get_inst_fmt(opcode_in) = FMT_R_TYPE else rf_rs1_data;
107
108     -- ALU input selection
109     alu_a <= operand1 when get_inst_fmt(opcode_in) = FMT_R_TYPE else operand2;
110     alu_b <= operand2 when get_inst_fmt(opcode_in) = FMT_R_TYPE else X"0000" &
        ↪  immediate_in;  -- Sign extend immediate
111     alu_c <= (others => '0');  -- Not used in current ISA
112
113     -- ALU instance
```

```
114     alu_inst: entity work.alu
115     port map (
116         rst      => rst,
117         a        => alu_a,
118         b        => alu_b,
119         c        => alu_c,
120         alu_op   => alu_op_in,
121         result   => alu_result,
122         zero     => alu_zero,
123         negative => alu_negative,
124         busy     => alu_busy,
125         valid    => alu_valid
126     );
127 
128     -- Branch logic
129     branch_logic: process(branch_in, opcode_in, alu_zero, alu_negative, operand1,
    ↪  immediate_in, pc_current)
130         variable target_offset : signed(31 downto 0);
131     begin
132         branch_condition <= '0';
133         branch_target <= (others => '0');
134 
135         if branch_in = '1' and inst_valid_in = '1' then
136             -- Sign extend immediate for branch offset
137             target_offset := resize(signed(immediate_in), 32);
138 
139             case opcode_in is
140                 when OP_JMP =>
141                     branch_condition <= '1';
142                     branch_target <= std_logic_vector(unsigned(pc_current) +
                        ↪  unsigned(target_offset(PC_WIDTH-1 downto 0)));
143 
144                 when OP_JZ =>
145                     if unsigned(operand1) = 0 then
146                         branch_condition <= '1';
147                         branch_target <= std_logic_vector(unsigned(pc_current) +
                            ↪  unsigned(target_offset(PC_WIDTH-1 downto 0)));
148                     end if;
149 
150                 when OP_JNZ =>
151                     if unsigned(operand1) /= 0 then
152                         branch_condition <= '1';
153                         branch_target <= std_logic_vector(unsigned(pc_current) +
                            ↪  unsigned(target_offset(PC_WIDTH-1 downto 0)));
154                     end if;
155 
156                 when OP_JLT =>
```

```
157                     if signed(operand1) < 0 then
158                         branch_condition <= '1';
159                         branch_target <= std_logic_vector(unsigned(pc_current) +
                            ↪ unsigned(target_offset(PC_WIDTH-1 downto 0)));
160                     end if;
161
162                 when OP_JGE =>
163                     if signed(operand1) >= 0 then
164                         branch_condition <= '1';
165                         branch_target <= std_logic_vector(unsigned(pc_current) +
                            ↪ unsigned(target_offset(PC_WIDTH-1 downto 0)));
166                     end if;
167
168                 when others =>
169                     null;
170             end case;
171         end if;
172     end process;
173
174     -- Output branch signals
175     pc_branch_taken <= branch_condition;
176     pc_branch_target <= branch_target;
177
178     -- Pipeline register
179     pipeline_reg: process(clk)
180     begin
181         if rising_edge(clk) then
182             if rst = '1' or flush = '1' then
183                 alu_result_reg <= (others => '0');
184                 mem_addr_reg <= (others => '0');
185                 mem_data_reg <= (others => '0');
186                 rd_addr_reg <= (others => '0');
187                 reg_write_en_reg <= '0';
188                 mem_read_reg <= '0';
189                 mem_write_reg <= '0';
190                 thread_id_reg <= 0;
191                 inst_valid_reg <= '0';
192                 halt_reg <= '0';
193             elsif stall = '0' and alu_busy = '0' then
194                 if opcode_in = OP_HALT then
195                     halt_reg <= '1';
196                 end if;
197
198                 -- ALU result for most operations
199                 alu_result_reg <= alu_result;
200
201                 -- Memory address calculation (base + offset)
```

```
202                 mem_addr_reg <= alu_result;  -- ALU calculates effective address
203
204                 -- Store data comes from rd (always in operand 1)
205                 mem_data_reg <= operand1;
206
207                 -- Pass through control signals
208                 rd_addr_reg <= rd_addr_in;
209                 reg_write_en_reg <= reg_write_en_in and inst_valid_in;
210                 --if reg_write_en_in = '1' then
211                    --report "opcode_in: " & integer'image(to_integer(unsigned(opcode_in)));
212                     --report "rd_addr_in: " &
                        ↪  integer'image(to_integer(unsigned(rd_addr_in)));
213                     --report "rs1_addr_in: " &
                        ↪  integer'image(to_integer(unsigned(rs1_addr_in)));
214                     --report "rs2_addr_in: " &
                        ↪  integer'image(to_integer(unsigned(rs2_addr_in)));
215                     --report "rf_rs1_data: " & to_hstring(rf_rs1_data);
216                     --report "rf_rs2_data: " & to_hstring(rf_rs2_data);
217                     --report "rf_rd_data: " & to_hstring(rf_rd_data);
218                     --report "operand1: " & to_hstring(operand1);
219                     --report "operand2: " & to_hstring(operand2);
220                     --report "reg_write_en_in: " & std_logic'image(reg_write_en_in);
221                     --report "alu_result: " & to_hstring(alu_result);
222                     --report "inst_valid_in: " & std_logic'image(inst_valid_in);
223                 --end if;
224                 mem_read_reg <= mem_read_in and inst_valid_in;
225                 mem_write_reg <= mem_write_in and inst_valid_in;
226                 thread_id_reg <= thread_id_in;
227                 inst_valid_reg <= inst_valid_in;
228             end if;
229         end if;
230     end process;
231
232     -- Output assignments
233     alu_result_out <= alu_result_reg;
234     mem_addr_out <= mem_addr_reg;
235     mem_data_out <= mem_data_reg;
236     rd_addr_out <= rd_addr_reg;
237     reg_write_en_out <= reg_write_en_reg;
238     mem_read_out <= mem_read_reg;
239     mem_write_out <= mem_write_reg;
240     thread_id_out <= thread_id_reg;
241     inst_valid_out <= inst_valid_reg;
242     halt_out <= halt_reg;
243
244 end architecture rtl;
```

## A.9 ALU Implementation

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use IEEE.MATH_REAL.ALL;
use work.types_pkg.all;
use work.isa_pkg.all;
-- Add ieee_proposed library for floating point
library ieee_proposed;
use ieee_proposed.fixed_float_types.all;
use ieee_proposed.fixed_pkg.all;
use ieee_proposed.float_pkg.all;

entity alu is
    port (
        rst         : in  std_logic;

        -- Operands
        a           : in  reg_data_t;
        b           : in  reg_data_t;
        c           : in  reg_data_t;  -- For MULACC

        -- Control (now 6 bits instead of 4)
        alu_op      : in  std_logic_vector(5 downto 0);

        -- Result
        result      : out reg_data_t;
        zero        : out std_logic;
        negative    : out std_logic;

        -- Multicycle operations
        busy        : out std_logic;
        valid       : out std_logic
    );
end entity alu;

architecture rtl of alu is
    -- Internal signals
    signal result_internal : std_logic_vector(DATA_WIDTH-1 downto 0);
    signal zero_internal   : std_logic;
    signal negative_internal : std_logic;
begin
    -- Main ALU process
    alu_proc: process(rst, a, b, c, alu_op)
        variable v_result : signed(DATA_WIDTH-1 downto 0);
        variable v_temp   : signed(DATA_WIDTH downto 0);
```

```
46          variable v_mul_temp : signed(2*DATA_WIDTH-1 downto 0);  -- For multiplication
47          -- Float32 variables for floating point operations
48          variable fa, fb, fresult : float32;
49          variable real_temp : real;
50          variable int_temp : integer;
51      begin
52          if rst = '1' then
53              result_internal <= (others => '0');
54              zero_internal <= '1';
55              negative_internal <= '0';
56              valid <= '0';
57          else
58              -- Default
59              valid <= '1';  -- Most operations complete in 1 cycle
60
61              case alu_op is
62                  -- Integer operations
63                  when ALU_ADD =>
64                      v_temp := resize(signed(a), DATA_WIDTH+1) + resize(signed(b),
                        ↪  DATA_WIDTH+1);
65                      v_result := v_temp(DATA_WIDTH-1 downto 0);
66
67                  when ALU_SUB =>
68                      v_temp := resize(signed(a), DATA_WIDTH+1) - resize(signed(b),
                        ↪  DATA_WIDTH+1);
69                      v_result := v_temp(DATA_WIDTH-1 downto 0);
70
71                  when ALU_MUL =>
72                      v_mul_temp := signed(a) * signed(b);
73                      v_result := v_mul_temp(DATA_WIDTH-1 downto 0);
74
75                  when ALU_DIV =>
76                      if signed(b) = 0 then
77                          -- Division by zero - return maximum value
78                          v_result := (others => '1');
79                      else
80                          v_result := signed(a) / signed(b);
81                      end if;
82
83                  when ALU_MOD =>
84                      if signed(b) = 0 then
85                          -- Modulo by zero - return zero
86                          v_result := (others => '0');
87                      else
88                          v_result := signed(a) mod signed(b);
89                      end if;
90
```

```
91                  when ALU_AND =>
92                      v_result := signed(a and b);
93
94                  when ALU_OR =>
95                      v_result := signed(a or b);
96
97                  when ALU_XOR =>
98                      v_result := signed(a xor b);
99
100                 when ALU_SHL =>
101                     v_result := shift_left(signed(a), to_integer(unsigned(b(4 downto 0))));
102
103                 when ALU_SHR =>
104                    v_result := shift_right(signed(a), to_integer(unsigned(b(4 downto 0))));
105
106                 when ALU_CMPLT =>
107                     if signed(a) < signed(b) then
108                         v_result := to_signed(1, DATA_WIDTH);
109                     else
110                         v_result := to_signed(0, DATA_WIDTH);
111                     end if;
112
113                 when ALU_CMPNE =>
114                     if a /= b then
115                         v_result := to_signed(1, DATA_WIDTH);
116                     else
117                         v_result := to_signed(0, DATA_WIDTH);
118                     end if;
119
120                 when ALU_MAX =>
121                     if signed(a) > signed(b) then
122                         v_result := signed(a);
123                     else
124                         v_result := signed(b);
125                     end if;
126
127                 when ALU_NEG =>
128                     v_result := -signed(a);
129
130                 when ALU_PASS_A =>
131                     v_result := signed(a);
132
133                 when ALU_PASS_B =>
134                     v_result := signed(b);
135
136                 -- Floating point operations
137                 when ALU_FADD =>
138                     fa := to_float(a, float32'high, -float32'low);
```

```
139                     fb := to_float(b, float32'high, -float32'low);
140                     fresult := fa + fb;
141                     v_result := signed(to_slv(fresult));
142
143                 when ALU_FSUB =>
144                     fa := to_float(a, float32'high, -float32'low);
145                     fb := to_float(b, float32'high, -float32'low);
146                     fresult := fa - fb;
147                     v_result := signed(to_slv(fresult));
148
149                 when ALU_FMUL =>
150                     fa := to_float(a, float32'high, -float32'low);
151                     fb := to_float(b, float32'high, -float32'low);
152                     fresult := fa * fb;
153                     v_result := signed(to_slv(fresult));
154                     if std_logic_vector(v_result) = x"7F800000" then
155                         report "NAN value produced in alu from a: " & to_hstring(a) & ", b:
                            ↪  " & to_hstring(b);
156                     end if;
157
158                 when ALU_FDIV =>
159                     fa := to_float(a, float32'high, -float32'low);
160                     fb := to_float(b, float32'high, -float32'low);
161                     fresult := fa / fb;
162                     v_result := signed(to_slv(fresult));
163
164                 when ALU_FSQRT =>
165                     fa := to_float(a, float32'high, -float32'low);
166                     fresult := sqrt(fa);
167                     v_result := signed(to_slv(fresult));
168
169                 when ALU_FRECIP =>
170                     fa := to_float(a, float32'high, -float32'low);
171                     fresult := reciprocal(fa);
172                     v_result := signed(to_slv(fresult));
173
174                 when ALU_FEXP2 =>
175                     -- Lacks implementation in VHDL 2008 support library
176                     null;
177
178                 when ALU_FLOG2 =>
179                     -- Lacks implementation in VHDL 2008 support library
180                     null;
181
182                 when ALU_FMAX =>
183                     fa := to_float(a, float32'high, -float32'low);
184                     fb := to_float(b, float32'high, -float32'low);
185                     fresult := maximum(fa, fb);
```

```
186                 v_result := signed(to_slv(fresult));
187
188             when ALU_FNEG =>
189                 fa := to_float(a, float32'high, -float32'low);
190                 fresult := -fa;
191                 v_result := signed(to_slv(fresult));
192
193             when ALU_FNE =>
194                 -- Float not equal comparison
195                 fa := to_float(a, float32'high, -float32'low);
196                 fb := to_float(b, float32'high, -float32'low);
197                 if fa /= fb then
198                     v_result := to_signed(1, DATA_WIDTH);
199                 else
200                     v_result := to_signed(0, DATA_WIDTH);
201                 end if;
202
203             when ALU_FLT =>
204                 -- Float less than comparison
205                 fa := to_float(a, float32'high, -float32'low);
206                 fb := to_float(b, float32'high, -float32'low);
207                 if fa < fb then
208                     v_result := to_signed(1, DATA_WIDTH);
209                 else
210                     v_result := to_signed(0, DATA_WIDTH);
211                 end if;
212
213             when ALU_FTOI =>
214                 -- Float to signed integer
215                 fa := to_float(a, float32'high, -float32'low);
216                 v_result := to_signed(fa, DATA_WIDTH);
217
218             when ALU_FTOUI =>
219                 -- Float to unsigned integer (stored in signed result)
220                 fa := to_float(a, float32'high, -float32'low);
221                 v_result := signed(std_logic_vector(to_unsigned(fa, DATA_WIDTH)));
222
223             when ALU_ITOF =>
224                 -- Signed integer to float
225                 fresult := to_float(signed(a), float32'high, -float32'low);
226                 v_result := signed(to_slv(fresult));
227
228             when ALU_UITOF =>
229                 -- Unsigned integer to float
230                 fresult := to_float(unsigned(a), float32'high, -float32'low);
231                 v_result := signed(to_slv(fresult));
232
233             when others =>
```

```
                    v_result := (others => '0');
            end case;

            -- Update result
            result_internal <= std_logic_vector(v_result);

            -- Update flags
            if v_result = 0 then
                zero_internal <= '1';
            else
                zero_internal <= '0';
            end if;

            negative_internal <= v_result(DATA_WIDTH-1);
        end if;
    end process;

    -- Output assignments
    result   <= result_internal;
    zero     <= zero_internal;
    negative <= negative_internal;
    busy     <= '0';  -- No multi-cycle operations in this simple version

end architecture rtl;
```

## A.10 Memory Stage

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use work.types_pkg.all;
use work.isa_pkg.all;

entity memory_stage is
    port (
        clk             : in  std_logic;
        rst             : in  std_logic;

        -- From execute stage
        alu_result_in   : in  reg_data_t;
        mem_addr_in     : in  reg_data_t;
        mem_data_in     : in  reg_data_t;
        rd_addr_in      : in  reg_addr_t;

        -- Control signals from execute
        reg_write_en_in : in  std_logic;
```

```
        mem_read_in     : in  std_logic;
        mem_write_in    : in  std_logic;

        -- Thread info
        thread_id_in    : in  thread_id_t;
        inst_valid_in   : in  std_logic;

        -- Outputs to writeback stage
        wb_data_out     : out reg_data_t;
        rd_addr_out     : out reg_addr_t;
        reg_write_en_out: out std_logic;

        -- Thread info passthrough
        thread_id_out   : out thread_id_t;
        inst_valid_out  : out std_logic;

        -- Forwarding output (for hazard handling)
        fwd_data        : out reg_data_t;
        fwd_addr        : out reg_addr_t;
        fwd_valid       : out std_logic;

        -- Shared memory interface (connected externally)
        mem_addr_out    : out std_logic_vector(SHARED_MEM_ADDR_WIDTH-1 downto 0);
        mem_data_out    : out std_logic_vector(31 downto 0);
        mem_we_out      : out std_logic;
        mem_re_out      : out std_logic;
        mem_read_data_in     : in  std_logic_vector(31 downto 0);
        mem_op_complete : in  std_logic;
        mem_op_stall    : in  std_logic;

        -- Pipeline control
        stall           : in  std_logic;
        flush           : in  std_logic;
        stall_out       : out std_logic  -- Memory stage can cause stalls
    );
end entity memory_stage;

architecture rtl of memory_stage is
begin
    -- Single process for everything
    main_process: process(clk)
        -- State type
        type mem_state_t is (IDLE, WAIT_MEM, COMPLETE);
        variable mem_state : mem_state_t := IDLE;

        -- Pipeline registers
        variable alu_result_reg   : reg_data_t := (others => '0');
        variable rd_addr_reg      : reg_addr_t := (others => '0');
```

```
68          variable reg_write_en_reg : std_logic := '0';
69          variable thread_id_reg    : thread_id_t := 0;
70          variable inst_valid_reg   : std_logic := '0';
71          variable mem_read_reg     : std_logic := '0';
72
73          -- Helper variables
74          variable v_result_data    : reg_data_t;
75          variable v_mem_op_active  : boolean;
76
77      begin
78          if rising_edge(clk) then
79              if rst = '1' then
80                  -- Reset state
81                  mem_state := IDLE;
82                  alu_result_reg := (others => '0');
83                  rd_addr_reg := (others => '0');
84                  reg_write_en_reg := '0';
85                  thread_id_reg := 0;
86                  inst_valid_reg := '0';
87                  mem_read_reg := '0';
88
89                  -- Clear outputs
90                  wb_data_out <= (others => '0');
91                  rd_addr_out <= (others => '0');
92                  reg_write_en_out <= '0';
93                  thread_id_out <= 0;
94                  inst_valid_out <= '0';
95                  fwd_data <= (others => '0');
96                  fwd_addr <= (others => '0');
97                  fwd_valid <= '0';
98                  mem_addr_out <= (others => '0');
99                  mem_data_out <= (others => '0');
100                 mem_we_out <= '0';
101                 mem_re_out <= '0';
102                 stall_out <= '0';
103
104             elsif flush = '1' then
105                 -- Flush pipeline
106                 mem_state := IDLE;
107                 inst_valid_reg := '0';
108                 reg_write_en_reg := '0';
109
110                 -- Clear outputs
111                 wb_data_out <= (others => '0');
112                 rd_addr_out <= (others => '0');
113                 reg_write_en_out <= '0';
114                 inst_valid_out <= '0';
115                 fwd_valid <= '0';
```

```
116                 mem_we_out <= '0';
117                 mem_re_out <= '0';
118                 stall_out <= '0';
119 
120             else
121                 -- Default outputs
122                 stall_out <= '0';
123                 inst_valid_out <= '0';
124                 reg_write_en_out <= '0';
125 
126                 -- State machine
127                 case mem_state is
128                     when IDLE =>
129                         if stall = '0' then
130                             -- Capture inputs
131                             alu_result_reg := alu_result_in;
132                             rd_addr_reg := rd_addr_in;
133                             reg_write_en_reg := reg_write_en_in and inst_valid_in;
134                             thread_id_reg := thread_id_in;
135                             inst_valid_reg := inst_valid_in;
136                             mem_read_reg := mem_read_in;
137 
138                             -- Check if memory operation is needed
139                             v_mem_op_active := inst_valid_in = '1' and (mem_read_in = '1' or
                                ↪  mem_write_in = '1');
140 
141                             if v_mem_op_active then
142                                 -- Setup memory operation
143                                 mem_addr_out <= mem_addr_in(SHARED_MEM_ADDR_WIDTH-1 downto 0);
144                                 mem_data_out <= mem_data_in;
145                                 mem_we_out <= mem_write_in;
146                                 if mem_write_in = '1' then
147                                     report "initiating mem write on thread " &
                                        ↪  integer'image(thread_id_in);
148                                     report "MEM mem_data_out: " & to_hstring(mem_data_in);
149                                     report "MEM mem_addr_out: " & integer'image(to_integer(
                                        ↪  unsigned(mem_addr_in(SHARED_MEM_ADDR_WIDTH-1
                                        ↪  downto 0))));
150                                 end if;
151                                 if mem_read_reg = '1' then
152                                     report "initiating mem read on thread " &
                                        ↪  integer'image(thread_id_in);
153                                 end if;
154                                 mem_re_out <= mem_read_in;
155                                 stall_out <= '1';
156                                 mem_state := WAIT_MEM;
157                             else
```

```
158                         mem_we_out <= '0';
159                         mem_re_out <= '0';
160                         -- No memory operation, pass through
161                         if inst_valid_reg = '1' then
162                             -- report "MEM: PASSING THROUGH ALU RES";
163                           -- report "MEM: alu_result_in: " & integer'image(to_int
                               ↪  eger(unsigned(alu_result_in)));
164                           -- report "MEM: alu_result_reg: " & integer'image(to_in
                               ↪  teger(unsigned(alu_result_reg)));
165                             wb_data_out <= alu_result_reg;
166                             rd_addr_out <= rd_addr_reg;
167                             reg_write_en_out <= reg_write_en_reg;
168                             thread_id_out <= thread_id_reg;
169                             inst_valid_out <= '1';
170                         end if;
171                     end if;
172                 end if;
173 
174                 when WAIT_MEM =>
175                     -- Wait for memory operation to complete
176                     if mem_op_complete = '1' then
177                         mem_we_out <= '0';
178                         mem_re_out <= '0';
179 
180                         mem_state := COMPLETE;
181                     else
182                         stall_out <= '1';
183                     end if;
184 
185                 when COMPLETE =>
186                     -- Output results
187                     if thread_id_in < 8 then
188                         report "completing mem op on thread: " &
                             ↪  integer'image(thread_id_in);
189                     end if;
190                     if mem_read_reg = '1' then
191                         report "mem read: " & to_hstring(mem_read_data_in);
192                         v_result_data := mem_read_data_in;
193                     else
194                         v_result_data := alu_result_reg;
195                     end if;
196 
197                     wb_data_out <= v_result_data;
198                     rd_addr_out <= rd_addr_reg;
199                     reg_write_en_out <= reg_write_en_reg;
200                     thread_id_out <= thread_id_reg;
201                     inst_valid_out <= '1';
```

```
202
203                         -- Return to IDLE
204                         mem_state := IDLE;
205
206                 end case;
207
208                 -- Forwarding logic (independent of state machine)
209                 fwd_valid <= '0';
210                 if reg_write_en_reg = '1' and inst_valid_reg = '1' then
211                     if mem_read_reg = '0' then
212                         -- ALU result is available immediately
213                         fwd_data <= alu_result_reg;
214                         fwd_addr <= rd_addr_reg;
215                         fwd_valid <= '1';
216                     elsif mem_state = COMPLETE then
217                         -- Memory read result is now available
218                         fwd_data <= mem_data_in;
219                         fwd_addr <= rd_addr_reg;
220                         fwd_valid <= '1';
221                     end if;
222                 end if;
223
224             end if;
225         end if;
226     end process;
227
228 end architecture rtl;
```

## A.11 Writeback Stage

```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  use IEEE.NUMERIC_STD.ALL;
4  use work.types_pkg.all;
5
6  entity writeback_stage is
7      port (
8          clk             : in  std_logic;
9          rst             : in  std_logic;
10
11         -- From memory stage
12         wb_data_in      : in  reg_data_t;
13         rd_addr_in      : in  reg_addr_t;
14         reg_write_en_in : in  std_logic;
15
16         -- Thread info
```

```
        thread_id_in    : in  thread_id_t;
        inst_valid_in   : in  std_logic;

        -- Register file interface
        rf_wr_enable    : out std_logic;
        rf_wr_addr      : out reg_addr_t;
        rf_wr_data      : out reg_data_t;
        rf_thread_id    : out thread_id_t;

        -- Forwarding output (for hazard handling)
        fwd_data        : out reg_data_t;
        fwd_addr        : out reg_addr_t;
        fwd_valid       : out std_logic;

        -- Pipeline control
        stall           : in  std_logic;
        flush           : in  std_logic;
        inst_valid_out  : out std_logic
    );
end entity writeback_stage;

architecture rtl of writeback_stage is
begin
    -- Single process for everything
    main_process: process(clk)
        -- Variables for cleaner code
        variable v_write_enable : std_logic;
        variable v_write_addr   : reg_addr_t;
        variable v_write_data   : reg_data_t;
        variable v_thread_id    : thread_id_t;

    begin
        if rising_edge(clk) then
            if rst = '1' then
                -- Reset all outputs
                rf_wr_enable <= '0';
                rf_wr_addr   <= (others => '0');
                rf_wr_data   <= (others => '0');
                rf_thread_id <= 0;
                fwd_data     <= (others => '0');
                fwd_addr     <= (others => '0');
                fwd_valid    <= '0';
                inst_valid_out <= '0';

            elsif flush = '1' then
                -- Flush pipeline - clear write enable to prevent invalid writes
                rf_wr_enable <= '0';
                fwd_valid    <= '0';
```

```
65
66              elsif stall = '0' then
67                  -- Normal operation - capture inputs
68                  v_write_enable := reg_write_en_in and inst_valid_in;
69                  v_write_addr   := rd_addr_in;
70                  v_write_data   := wb_data_in;
71                  v_thread_id    := thread_id_in;
72
73                  -- Drive register file write interface
74                  rf_wr_enable <= v_write_enable;
75                  rf_wr_addr   <= v_write_addr;
76                  rf_wr_data   <= v_write_data;
77                  rf_thread_id <= v_thread_id;
78
79                  if (v_write_enable = '1') then
80                     -- report "WB: writing data " & to_hstring(v_write_data);
81                  end if;
82
83                  inst_valid_out <= inst_valid_in;
84
85                  -- Drive forwarding interface
86                  -- Data is available for forwarding in the same cycle
87                  fwd_data  <= v_write_data;
88                  fwd_addr  <= v_write_addr;
89                  fwd_valid <= v_write_enable;
90
91              else
92                  -- Stalled - hold current state
93                  -- Clear write enable to prevent repeated writes
94                  rf_wr_enable <= '0';
95                  -- Keep forwarding active if it was valid
96                  -- (forwarding should remain available during stalls)
97              end if;
98          end if;
99      end process;
100
101 end architecture rtl;
```

# B Appendix B: Tinygrad Backend Extensions

## B.1 Rivyera Backend

```
1 from typing import Optional, Any, TYPE_CHECKING
2 import pickle, base64, itertools, time, struct, sys, os
3 import ctypes
```

```
from tinygrad.dtype import DType, dtypes, ImageDType, PtrDType, truncate
from tinygrad.helpers import all_same, getenv, flatten, get_single_element, DEBUG
from tinygrad.device import Compiled, Compiler, Allocator, BufferSpec
from tinygrad.ops import exec_alu, Ops, UOp, UPat, GroupOp, PatternMatcher
from tinygrad.codegen.devectorizer import no_vectorized_alu
from tinygrad.renderer import Renderer
import functools
from tinygrad.runtime.support.compiler_rivyera import RivyeraCompiler
from tinygrad.runtime.autogen.rivyera import (
    se_getMachineCount, se_allocMachine, se_freeMachine, se_read, se_write, se_flush,
    se_getSlotCount, se_getFPGACount, se_waitForData, se_program, se_deprogram,
    struct__SE_OPTIONS_T, struct__SE_ADDR, se_routing_normal, se_write_sync,
    ↪ se_write_async,
    SE_STATUS, SeApiSuccess, SeReadActive, SeReadPassive, se_time_t, SE_ADDR_FPGA_ALL,
    ↪ SE_ADDR_SLOT_ALL, size_t,
    se_getControllerInfo, struct__SE_CONTROLLERINFO
)

# Command constants for FPGA communication
CMD_READ = 0x01   # Read data from FPGA buffer
CMD_WRITE = 0x02  # Write data to FPGA buffer
CMD_EXECUTE = 0x03       # Execute computation on FPGA
CMD_STATUS = 0x04        # Query execution status
CMD_LOAD_KERNEL = 0x05 # Load kernel onto FPGA

EXECUTION_STATUS_NOT_COMPLETED = 0x00
EXECUTION_STATUS_COMPLETED = 0x01

# Status codes for FPGA responses (simplified)
STATUS_OK = 0x01         # Operation completed successfully
STATUS_ERROR = 0xFF      # Operation failed

class RivyeraRenderer(Renderer):
    device = "RIVYERA"
    supports_float4 = False
    has_local=False

    # Add extra_matcher to force devectorization
    extra_matcher = PatternMatcher([
        # Force all ALU operations to be devectorized
        (UPat((*GroupOp.ALU, Ops.CAST, Ops.BITCAST, Ops.ASSIGN), name="alu"),
        ↪ no_vectorized_alu),
        # Force WHERE operations to be devectorized
        (UPat(Ops.WHERE, name="alu"), no_vectorized_alu),
    ])

    def render(self, uops: list[UOp]) -> str:
```

```
48          # Simplified: only encode UOps for the compiler
49          return base64.b64encode(pickle.dumps(uops)).decode()
50
51  class RivyeraProgram:
52      def __init__(self, dev:'RivyeraDevice', name:str, lib:bytes):
53          self.dev = dev
54          self.lib = lib
55          self.name = name
56
57      def __call__(self, *bufs, global_size=(1,1,1), local_size=(1,1,1), vals=(),
        ↪  wait=False):
58          # Execute on FPGA cluster via Rivyera API
59          cores_enabled = local_size[0]
60          return self.dev.rivyera_execute(self.lib, bufs, vals, cores_enabled=cores_enabled,
            ↪  wait=wait)
61
62  # TODO create class for allocated buffers (refactor)
63  # TODO create function for sending out commands (refactor)
64
65  class RivyeraAllocator(Allocator):
66      def __init__(self, dev:'RivyeraDevice'):
67          self.dev = dev
68          self.allocated_buffers = {}  # Track allocated buffers: buf_id -> {address, size,
            ↪  fpga_slot, fpga_num}
69          self.free_segments = []      # List of free memory segments: [(address, size), ...]
70          self.next_buffer_id = 0      # Next buffer ID to assign
71
72          # Initialize with a single large free segment (e.g., 256KB of BRAM)
73          TOTAL_MEMORY_SIZE = 256 * 1024  # 256KB
74          self.free_segments.append((0, TOTAL_MEMORY_SIZE))
75
76          super().__init__()
77
78      def _alloc(self, size, options=None):
79          # Allocate memory on the FPGA cluster
80          buf_id = self.rivyera_alloc_memory(size)
81          return buf_id
82
83      def _free(self, opaque, options:BufferSpec):
84          # Free allocated memory
85          self.rivyera_free_memory(opaque)
86
87      def _copyin(self, dest, src: memoryview):
88          # Copy from host to device
89          self.rivyera_copy_to_device(dest, src, len(src))
90
91      def _copyout(self, dest: memoryview, src):
```

```
92          # Copy from device to host
93          self.rivyera_copy_from_device(dest, src, len(dest))
94
95      def rivyera_alloc_memory(self, size):
96          # Round up size to 8-byte boundary
97          aligned_size = (size + 7) & ~7
98
99          # Find the smallest free segment that can fit the requested size
100         suitable_segments = []
101         for i, (addr, seg_size) in enumerate(self.free_segments):
102             # Calculate aligned address within this segment
103             aligned_addr = (addr + 7) & ~7
104             # Calculate how much space we lose due to alignment
105             alignment_waste = aligned_addr - addr
106             # Check if we still have enough space after alignment
107             if seg_size >= aligned_size + alignment_waste:
108                 suitable_segments.append((i, addr, seg_size, aligned_addr, alignment_waste))
109
110         if not suitable_segments:
111             raise RuntimeError(f"Out of memory: cannot allocate {size} bytes (aligned to
                ↪  {aligned_size} bytes)")
112
113         # Sort by effective size (segment size minus alignment waste) to get the smallest
            ↪  suitable segment
114         suitable_segments.sort(key=lambda x: x[2] - x[4])
115         segment_idx, segment_addr, segment_size, aligned_addr, alignment_waste =
            ↪  suitable_segments[0]
116
117         # Remove the segment from free list
118         self.free_segments.pop(segment_idx)
119
120         # Handle fragments before and after the allocation
121         fragments = []
122
123         # Fragment before the aligned allocation (due to alignment)
124         if alignment_waste > 0:
125             fragments.append((segment_addr, alignment_waste))
126
127         # Fragment after the allocation
128         used_space = alignment_waste + aligned_size
129         if segment_size > used_space:
130             remainder_addr = segment_addr + used_space
131             remainder_size = segment_size - used_space
132             fragments.append((remainder_addr, remainder_size))
133
134         # Add fragments back to free list
135         self.free_segments.extend(fragments)
```

```
136
137         # Create address for command
138         addr = self._create_addr()
139
140         # Allocate buffer ID and track the allocation
141         buf_id = self.next_buffer_id
142         self.allocated_buffers[buf_id] = {
143             "address": aligned_addr,
144             "size": aligned_size,  # Store the aligned size
145             "fpga_slot": addr.slot,
146             "fpga_num": addr.fpga
147         }
148
149         self.next_buffer_id += 1
150         return buf_id
151
152     def rivyera_free_memory(self, buf_id):
153         # Free a buffer on the FPGA
154         if buf_id not in self.allocated_buffers:
155             return
156
157         buffer_info = self.allocated_buffers[buf_id]
158
159         # Add the freed memory back to the free segments list
160         self.free_segments.append((buffer_info["address"], buffer_info["size"]))
161
162         # Merge adjacent free segments to reduce fragmentation
163         self._merge_free_segments()
164
165         # Remove from tracking
166         del self.allocated_buffers[buf_id]
167
168     def _merge_free_segments(self):
169         """Merge adjacent free segments to reduce fragmentation"""
170         if len(self.free_segments) <= 1:
171             return
172
173         # Sort segments by address
174         self.free_segments.sort(key=lambda x: x[0])
175
176         # Merge adjacent segments
177         merged = []
178         current_addr, current_size = self.free_segments[0]
179
180         for addr, size in self.free_segments[1:]:
181             if current_addr + current_size == addr:
182                 # Adjacent segments, merge them
183                 current_size += size
```

```
            else:
                # Non-adjacent, save current and start new
                merged.append((current_addr, current_size))
                current_addr, current_size = addr, size

        # Don't forget the last segment
        merged.append((current_addr, current_size))

        self.free_segments = merged

    def rivyera_copy_to_device(self, dest_id, src, size):
        # Copy data from host to device buffer
        if dest_id not in self.allocated_buffers:
            raise ValueError(f"Invalid buffer ID: {dest_id}")

        buffer_info = self.allocated_buffers[dest_id]

        # Create address
        fpga_addr = self._create_addr(
            slot=buffer_info["fpga_slot"],
            fpga=buffer_info["fpga_num"]
        )

        # For simplicity, transfer in one go if small enough
        # Otherwise chunk it
        CHUNK_SIZE = 256  # 256 words = 2KB chunks

        dest_addr = buffer_info["address"]
        remaining = size
        offset = 0

        while remaining > 0:
            chunk_size = min(remaining, CHUNK_SIZE * 8)
            words_needed = (chunk_size + 7) // 8

            # Prepare command: CMD | buffer_id | offset | length | data...
            total_words = 4 + words_needed
            data = (ctypes.c_uint64 * total_words)()

            data[0] = CMD_WRITE
            data[1] = (dest_addr + offset) // 8
            data[2] = chunk_size   # Length in bytes
            data[3] = 0 # empty third param

            # Pack data
            src_bytes = bytes(src[offset:offset+chunk_size])
            for i in range(words_needed):
                word_data = 0
```

```
                for j in range(8):
                    if i*8+j < len(src_bytes):
                        word_data |= src_bytes[i*8+j] << (j*8)
                data[4+i] = word_data

            # Send command and data
            self._write_data(fpga_addr, data, total_words)

            # Wait for response
            time.sleep(0.01)
            response = (ctypes.c_uint64 * 1)()
            self._read_data_passive(fpga_addr, response, 1)

            if response[0] != STATUS_OK:
                raise RuntimeError(f"Failed to write buffer to FPGA")

            offset += chunk_size
            remaining -= chunk_size

    def rivyera_copy_from_device(self, dest, src_id, size):
        # Copy data from device to host
        if src_id not in self.allocated_buffers:
            raise ValueError(f"Invalid buffer ID: {src_id}")

        buffer_info = self.allocated_buffers[src_id]

        # Create address
        addr = self._create_addr(
            slot=buffer_info["fpga_slot"],
            fpga=buffer_info["fpga_num"]
        )

        # Read in chunks
        CHUNK_SIZE = 256  # 256 words = 2KB chunks

        src_address = buffer_info["address"]
        offset = 0
        remaining = size

        while remaining > 0:
            chunk_size = min(remaining, CHUNK_SIZE * 8)
            words_needed = (chunk_size + 7) // 8

            # Send read command: CMD | buffer_id | offset | length
            cmd_data = (ctypes.c_uint64 * 4)()
            cmd_data[0] = CMD_READ
            cmd_data[1] = (src_address + offset) // 8
            cmd_data[2] = chunk_size   # Length in bytes
```

```
280             cmd_data[3] = 0 # empty third param
281
282             self._write_data(addr, cmd_data, 4)
283
284             # Read response: status + data
285             time.sleep(0.02)  # Give FPGA time to prepare data
286             response_words = 1 + words_needed
287             response = (ctypes.c_uint64 * response_words)()
288             self._read_data_passive(addr, response, response_words)
289
290             if response[0] != STATUS_OK:
291                 raise RuntimeError(f"Failed to read buffer from FPGA")
292
293             # Unpack data
294             for i in range(words_needed):
295                 word = response[i + 1]
296                 for j in range(8):
297                     if offset + i*8 + j < size:
298                         dest[offset + i*8 + j] = (word >> (j*8)) & 0xFF
299
300             offset += chunk_size
301             remaining -= chunk_size
302
303     def _create_addr(self, slot=None, fpga=None):
304         """Create an address structure for Rivyera"""
305         addr = struct__SE_ADDR()
306         addr.contr = 0
307         # Use device-specific slot and fpga if not provided
308         addr.slot = slot if slot is not None else self.dev.slot
309         addr.fpga = fpga if fpga is not None else self.dev.fpga_num
310         addr.reg = 0
311         return addr
312
313     def _write_data(self, addr, data, count):
314         """Write data array to Rivyera"""
315         timeout = se_time_t(10000)  # 10 second timeout
316         written = ctypes.c_uint64(0)
317         status = se_write(self.dev.machine_id, addr, data, count, ctypes.byref(written),
        ↪  timeout)
318
319         if status != SeApiSuccess:
320             raise RuntimeError(f"Failed to write data to FPGA, status: {status}")
321
322         # Flush to ensure data is sent
323         se_flush(self.dev.machine_id, addr.contr, timeout)
324
325     def _read_data_passive(self, addr, data, count):
326         """Read data using passive mode (no read request)"""
```

```
327         timeout = se_time_t(10000)  # 10 second timeout
328         read = ctypes.c_uint64(0)
329 
330         # Use passive read - just read what's already there
331         status = se_read(
332             self.dev.machine_id, addr, data, count,
333             SeReadPassive, ctypes.byref(read), timeout
334         )
335 
336         self.dev._total_words_read += count
337 
338         if status != SeApiSuccess or read.value != count:
339             raise RuntimeError(f"Failed to read data from FPGA, status: {status}, read:
    ↪  {read.value}/{count}")
340 
341 
342 class RivyeraDevice(Compiled):
343     # Add class-level tracking of all devices
344     devices: dict[str, 'RivyeraDevice'] = {}
345 
346     def __init__(self, device: str):
347         # Parse device string to get FPGA index (e.g., "RIVYERA:0", "RIVYERA:1")
348         parts = device.split(":")
349         self._total_words_read = 0
350         self.fpga_index = int(parts[1]) if len(parts) > 1 else 0
351 
352         # Initialize Rivyera resources
353         self.machine_count = se_getMachineCount()
354         if self.machine_count == 0:
355             raise RuntimeError("No Rivyera machines found")
356         self.driver_name = "isim" if os.getenv("RIVYERA_SIM", "0") == "1" else "pcie"
357         self.machine_id = self._get_machine_id()
358         if self.machine_id is False:
359             raise RuntimeError(f"Could not find machine id for RivyeraDevice with
    ↪  driver_name {self.driver_name}")
360 
361         # Setup options
362         self.options = struct__SE_OPTIONS_T()
363         self.options.write_behavior = se_write_sync
364         self.options.routing_method = se_routing_normal
365 
366         # Only allocate the machine once (shared across all FPGA instances)
367         if not RivyeraDevice.devices:
368             status = se_allocMachine(self.machine_id, ctypes.byref(self.options))
369             if status != SeApiSuccess:
370                 raise RuntimeError(f"Failed to allocate Rivyera machine, status: {status}")
371 
```

```
372         # Get hardware information
373         self.slot_count = ctypes.c_uint32(0)
374         status = se_getSlotCount(self.machine_id, ctypes.byref(self.slot_count))
375         if status != SeApiSuccess:
376             self._cleanup()
377             raise RuntimeError(f"Failed to get slot count, status: {status}")
378 
379         # Map available FPGAs
380         self.fpga_map = {}
381         total_fpgas = 0
382         for slot in range(self.slot_count.value):
383             fpga_count = ctypes.c_uint32(0)
384             status = se_getFPGACount(self.machine_id, slot, ctypes.byref(fpga_count))
385             if status == SeApiSuccess:
386                 self.fpga_map[slot] = fpga_count.value
387                 total_fpgas += fpga_count.value
388 
389         # Validate FPGA index
390         if self.fpga_index >= total_fpgas:
391             raise RuntimeError(f"FPGA index {self.fpga_index} out of range, only
                ↪ {total_fpgas} FPGAs available")
392 
393         # Calculate slot and fpga number from linear index
394         current_idx = 0
395         for slot, fpga_count in self.fpga_map.items():
396             if current_idx + fpga_count > self.fpga_index:
397                 self.slot = slot
398                 self.fpga_num = self.fpga_index - current_idx
399                 break
400             current_idx += fpga_count
401 
402         # Program the specific FPGA if it's the first device
403         if not RivyeraDevice.devices and os.getenv("RIVYERA_DELAY_FPGA_PROGRAM", "0") !=
            ↪ "1":
404             self._program_all_fpgas()
405 
406         # Add execution tracking
407         self.pending_executions: list[tuple[int, struct__SE_ADDR]] = []  # (execution_id,
            ↪ fpga_addr)
408         self.next_execution_id = 0
409 
410         # Track this device instance
411         RivyeraDevice.devices[device] = self
412 
413         # Initialize the base class with a device-specific allocator
414         super().__init__(device, RivyeraAllocator(dev=self), RivyeraRenderer(),
415                          RivyeraCompiler(), functools.partial(RivyeraProgram, self))
```

```
416
417     def synchronize(self):
418         """Wait for all pending operations on this FPGA to complete"""
419         allocator = self.allocator
420
421         # Poll all pending executions
422         for exec_id, addr in self.pending_executions:
423             # Poll until complete
424             while True:
425                 # Send status query
426                 cmd_data = (ctypes.c_uint64 * 4)()
427                 cmd_data[0] = CMD_STATUS
428                 cmd_data[1] = exec_id
429                 cmd_data[2] = 0
430                 cmd_data[3] = 0
431
432                 allocator._write_data(addr, cmd_data, 4)
433                 time.sleep(0.001)  # 1ms polling interval
434
435                 response = (ctypes.c_uint64 * 2)()
436                 allocator._read_data_passive(addr, response, 2)
437
438                 if response[0] == STATUS_OK and response[1] == EXECUTION_STATUS_COMPLETED:
439                     break
440                 elif response[0] == STATUS_ERROR:
441                     raise RuntimeError(f"Execution {exec_id} failed on FPGA")
442                 # Otherwise, still running - continue polling
443
444         # Clear pending executions
445         self.pending_executions.clear()
446
447     @staticmethod
448     def synchronize_system():
449         for d in RivyeraDevice.devices: d.synchronize()
450
451     def _program_all_fpgas(self):
452         """Program all FPGAs with the pre-compiled bitstream"""
453         programming_file_path = self._get_programming_file_path()
454
455         if not os.path.exists(programming_file_path):
456             raise FileNotFoundError(f"Bitstream file not found: {programming_file_path}")
457
458         # Program all FPGAs
459         for slot in range(self.slot_count.value):
460             addr = struct__SE_ADDR()
461             addr.contr = 0
462             addr.slot = slot
463             addr.fpga = SE_ADDR_FPGA_ALL
```

```
464             addr.reg = 0
465
466             timeout = se_time_t(60000)
467             status = se_program(self.machine_id, addr, programming_file_path.encode(),
                ↪  timeout)
468
469             if status != SeApiSuccess:
470                 self._cleanup()
471                 raise RuntimeError(f"Failed to program FPGAs on slot {slot}, status:
                    ↪  {status}")
472
473         print(f"Successfully programmed all FPGAs")
474         time.sleep(2.0)
475
476     def _get_programming_file_path(self):
477         """Get correct programming file path depending on if we are using isim or pcie"""
478         programming_file = "rivyera_accelerator.sim" if self.driver_name == "isim" else
            ↪  "rivyera_accelerator_top.bit"
479         return os.path.join(
480             os.path.dirname(os.path.dirname(os.path.dirname(os.path.abspath(__file__)))),
481             "rivyera-accelerator", "fpga", "vhdl", programming_file
482         )
483
484     def _get_machine_id(self):
485         """Get correct machine_id depending on if we are using sim or pcie"""
486         for machine_id in range(self.machine_count):
487             controller_info = struct__SE_CONTROLLERINFO()
488             status = se_getControllerInfo(machine_id, 0, ctypes.byref(controller_info))
489             if status != SeApiSuccess:
490                 raise RuntimeError(f"Failed to fetch controller info for machine id
                    ↪  {machine_id}, status: {status}")
491             if ctypes.cast(controller_info.driver_name, ctypes.c_char_p).value.decode() ==
                ↪  self.driver_name:
492                 return machine_id
493         return False
494
495     def _cleanup(self):
496         # Free the machine if it was allocated
497         if hasattr(self, 'machine_id'):
498             # Deprogram FPGAs if they were programmed
499             if hasattr(self, 'fpga_map'):
500                 addr = struct__SE_ADDR()
501                 addr.contr = 0
502                 addr.slot = 0
503                 addr.fpga = SE_ADDR_FPGA_ALL
504                 addr.reg = 0
505                 se_deprogram(self.machine_id, addr)
```

```
506
507             se_freeMachine(self.machine_id)
508
509     def __del__(self):
510         self._cleanup()
511
512     def _load_kernel(self, lib:bytes):
513         allocator = self.allocator
514
515         # Create address
516         fpga_addr = struct__SE_ADDR()
517         fpga_addr.contr = 0
518         fpga_addr.slot = self.slot
519         fpga_addr.fpga = self.fpga_num
520         fpga_addr.reg = 0
521
522         # Write kernel into memory
523         buf_id = allocator._alloc(len(lib))
524         allocator.rivyera_copy_to_device(buf_id, lib, len(lib))
525
526         # Send load kernel command
527         cmd_Data = cmd_data = (ctypes.c_uint64 * 4)()
528         cmd_Data[0] = CMD_LOAD_KERNEL # Cmd
529         cmd_Data[1] = allocator.allocated_buffers[buf_id]["address"] // 8 # Kernel address
        ↪  in 8-byte words
530         cmd_Data[2] = allocator.allocated_buffers[buf_id]["size"] # Kernel size in bytes
531         cmd_Data[3] = 0 # Empty third param
532
533         allocator._write_data(fpga_addr, cmd_data, 4)
534
535         # Read response
536         time.sleep(0.02)
537         response = (ctypes.c_uint64 * 1)()
538         allocator._read_data_passive(fpga_addr, response, 1)
539
540         if response[0] != STATUS_OK:
541                 raise RuntimeError(f"Failed to load kerrnel into FPGA")
542
543     def _patch_kernel(self, lib:bytes, bufs):
544         allocator = self.allocator
545         # Parse kernel header
546         offset = 0
547         magic = struct.unpack('<I', lib[offset:offset+4])[0]
548         offset += 4
549
550         if magic != 0xDEADBEEF:
551             raise RuntimeError("Invalid kernel format")
552
```

```
553         num_placeholders = struct.unpack('<I', lib[offset:offset+4])[0]
554         offset += 4
555 
556         # Read placeholder information
557         placeholders = []
558         for i in range(num_placeholders):
559             inst_idx, buf_idx, reg = struct.unpack('<III', lib[offset:offset+12])
560             placeholders.append((inst_idx, buf_idx, reg))
561             offset += 12
562 
563         # Instructions start after header
564         instructions_start = offset
565         instructions = bytearray(lib[instructions_start:])
566 
567         # Patch placeholders with actual buffer addresses
568         for inst_idx, buf_idx, reg in placeholders:
569             if buf_idx < len(bufs):
570                 buf_id = bufs[buf_idx]
571                 if buf_id in allocator.allocated_buffers:
572                     actual_addr = allocator.allocated_buffers[buf_id]["address"]
573                     # Since the system is adressed by 4-byte words, divide the address by 4
574                     word_addr = actual_addr // 4
575 
576                     # Create LOAD_IMM instruction with actual address
577                     # For now, load lower 16 bits (we'd need multiple instructions for full
                        ↪  address)
578                    patched_inst = (0x11 << 26) | (reg << 21) | (0 << 16) | (word_addr & 0xFFFF)
579 
580                     # Patch the instruction
581                     inst_offset = inst_idx * 4
582                     struct.pack_into('<I', instructions, inst_offset, patched_inst)
583                 else:
584                     raise RuntimeError(f"Buffer {buf_idx} not found in allocated buffers")
585             else:
586                 raise RuntimeError(f"Buffer index {buf_idx} out of range")
587 
588         patched_kernel = bytes(instructions)
589         return patched_kernel
590 
591     def rivyera_execute(self, lib:bytes, bufs, vals, cores_enabled=1, wait=False):
592         # Execute operations on specific FPGA
593         allocator = self.allocator
594 
595         # Get execution ID
596         exec_id = self.next_execution_id
597         self.next_execution_id += 1
598 
599         patched_kernel = self._patch_kernel(lib, bufs)
```

```
600
601         if DEBUG >= 2:
602             print("=" * 60)
603             print("PATCHED KERNEL DEBUG INFO:")
604             print(RivyeraCompiler.decode_and_display_instructions(patched_kernel,
                ↪  patched=True))
605             print("=" * 60)
606
607         # Use device-specific FPGA address
608         addr = struct__SE_ADDR()
609         addr.contr = 0
610         addr.slot = self.slot
611         addr.fpga = self.fpga_num
612         addr.reg = 0
613
614         # Load the patched kernel
615         self._load_kernel(lib=patched_kernel)
616
617         # Send execute command
618         cmd_data = (ctypes.c_uint64 * 4)()
619         cmd_data[0] = CMD_EXECUTE
620         cmd_data[1] = exec_id
621         cmd_data[2] = cores_enabled
622         cmd_data[3] = 0
623
624         allocator._write_data(addr, cmd_data, 4)
625
626         # Read response
627         time.sleep(0.02)
628         response = (ctypes.c_uint64 * 1)()
629         allocator._read_data_passive(addr, response, 1)
630
631         # Track this execution
632         self.pending_executions.append((exec_id, addr))
633
634         if wait:
635             return self.synchronize()
636
637         return response[0] == STATUS_OK
```

## B.2 Rivyera Compiler

```
1 from typing import Optional, Any, TYPE_CHECKING
2 from collections import defaultdict
3 import pickle, base64, struct
4 from tinygrad.dtype import DType, dtypes
```

```
from tinygrad.device import Compiler
from tinygrad.ops import Ops, UOp, GroupOp

class RivyeraCompiler(Compiler):
    def compile(self, src: str) -> bytes:
        uops = pickle.loads(base64.b64decode(src))

        # ISA definitions
        OPS = {
            # ALU
            (Ops.ADD, 'int'): 0x01, (Ops.SUB, 'int'): 0x02, (Ops.MUL, 'int'): 0x03, (Ops.IDIV, 'int'): 0x04,
            (Ops.MOD, None): 0x05, (Ops.SHL, None): 0x06, (Ops.SHR, None): 0x07,
            (Ops.AND, None): 0x08, (Ops.OR, None): 0x09, (Ops.XOR, None): 0x0A,
            (Ops.NEG, 'int'): 0x0B, (Ops.CMPLT, 'int'): 0x0C, (Ops.CMPNE, 'int'): 0x0D, (Ops.MAX, 'int'): 0x0E,
            # Float
            (Ops.ADD, 'float'): 0x12, (Ops.SUB, 'float'): 0x13, (Ops.MUL, 'float'): 0x14, (Ops.FDIV, 'float'): 0x15,
            (Ops.SQRT, 'float'): 0x16, (Ops.RECIP, 'float'): 0x17, (Ops.EXP2, 'float'): 0x18, (Ops.LOG2, 'float'): 0x19,
            (Ops.MAX, 'float'): 0x1A, (Ops.NEG, 'float'): 0x1B, (Ops.CMPNE, 'float'): 0x1C, (Ops.CMPLT, 'float'): 0x1D,
            # Cast
            (Ops.CAST, 'f2i'): 0x1E, (Ops.CAST, 'f2u'): 0x1F, (Ops.CAST, 'i2f'): 0x22, (Ops.CAST, 'u2f'): 0x23,
            # Memory/Control
            (Ops.LOAD, None): 0x20, (Ops.STORE, None): 0x21, (Ops.BARRIER, None): 0x3E, (Ops.NOOP, None): 0x3F,
        }
        (OP_PLACEHOLDER_BUFFER, OP_ADD, OP_SUB, OP_MUL, OP_DIV, OP_MOD, OP_SHL, OP_SHR,
        OP_AND, OP_OR, OP_XOR, OP_NEG, OP_CMPLT, OP_CMPNE, OP_MAX, OP_MOV, OP_LOAD_IMM,
        OP_FADD, OP_FSUB, OP_FMUL, OP_FDIV, OP_FSQRT, OP_FRECIP, OP_FEXP2, OP_FLOG2,
        OP_FMAX, OP_FNEG, OP_FNE, OP_FLT, OP_FTOI, OP_FTOUI, OP_ITOF, OP_UITOF,
        OP_LOAD, OP_STORE, OP_JMP, OP_JZ, OP_JNZ, OP_JLT, OP_JGE, OP_HALT, OP_BARRIER, OP_NOP) = (
        0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E,
        0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E,
        0x1F, 0x22, 0x23, 0x20, 0x21, 0x30, 0x31, 0x32, 0x33, 0x34, 0x3D, 0x3E, 0x3F)

        J_OPS = {OP_JMP, OP_JZ, OP_JNZ, OP_JLT, OP_JGE}

        # State
        insts = []
```

```
        ZERO_REG, TEMP_REG, SHIFT_REG, SPILL_REGA, SPILL_REGB, SPILL_REGC, SPILL_BASE,
        ↪  THREAD_ID = 0, 1, 2, 3, 4, 5, 30, 31
        SPILL_REGISTERS = [SPILL_REGA, SPILL_REGB, SPILL_REGC]
        RESERVED_REGISTERS = {ZERO_REG, TEMP_REG, SHIFT_REG, SPILL_REGA, SPILL_REGB,
        ↪  SPILL_REGC, SPILL_BASE, THREAD_ID}
        MAX_MEMORY, SPILL_PER_CORE = 2560, 512

        # Helpers
        encode = lambda op, rd=0, rs1=0, rs2=0, imm=0: (op << 26) | (rd << 21) | (rs1 << 16) |
        ↪  (rs2 << 11) | (imm & 0xFFFF)
        add_inst = lambda *args, **kwargs: insts.append(encode(*args, **kwargs)) or
        ↪  len(insts) - 1

        def get_op(uop):
            dt = 'float' if dtypes.is_float(uop.dtype) else 'int'
            if uop.op == Ops.CAST:
               src_f, dst_f = dtypes.is_float(uop.src[0].dtype), dtypes.is_float(uop.dtype)
                cat = 'f2u' if src_f and not dst_f and dtypes.is_unsigned(uop.dtype) else \
                      'f2i' if src_f and not dst_f else \
                     'u2f' if not src_f and dst_f and dtypes.is_unsigned(uop.src[0].dtype)
                     ↪  else \
                     'i2f' if not src_f and dst_f else None
                return OPS.get((Ops.CAST, cat), OP_MOV)
            return OPS.get((uop.op, dt), OPS.get((uop.op, None), 0))

        # Live range analysis of the uops
        live_start = {} # uop -> first declaration
        live_end = {} # uop -> last use
        for i, uop in enumerate(uops):
            live_start[uop] = i
            for src in uop.src: live_end[src] = i
        # Extend lifetimes for variables whose intervals are within a loop
        loop_ends = {}
        stack = []
        for i, uop in enumerate(uops):
            if uop.op is Ops.RANGE: stack.append(i)
            elif uop.op is Ops.ENDRANGE and stack:
                start = stack.pop()
                end = i
                loop_ends[start] = end
                for j in stack:
                    if j in loop_ends: loop_ends[j] = max(loop_ends[j], end)
        for i, uop in enumerate(uops):
            for start, end in loop_ends.items():
                if start <= i <= end:
                    for src in uop.src:
                        if src in live_end: live_end[src] = max(live_end[src], end)
```

```python
    # Global register allocation through the use of linear scan (Poletto, Sarkar)
    active_uops = set() # set of currently active uops
    registers = {} # uop -> register
    spill_locations = {} # uop -> stack location
    free_regs = set(range(32)) - RESERVED_REGISTERS
    next_spill_slot = 0
    def expire_old_intervals(i):
        for uop in sorted(list(active_uops), key=lambda uop: live_end[uop]):
            if live_end[uop] >= i:
                return
            active_uops.remove(uop)
            free_regs.add(registers[uop])

    def spill_at_interval(i):
        nonlocal next_spill_slot
        spill = sorted(list(active_uops), key=lambda uop: live_end[uop])[-1]
        if live_end[spill] > live_end[uops[i]]:
            registers[uops[i]] = registers[spill]
            spill_locations[spill] = next_spill_slot
            active_uops.remove(spill)
            active_uops.add(uops[i])
        else:
            spill_locations[uops[i]] = next_spill_slot
        next_spill_slot += 1

    # Allocate all the registers
    for i, uop in enumerate(uops):
        if uop.op in [Ops.STORE, Ops.ENDRANGE, Ops.BARRIER, Ops.SINK]:
            continue
        expire_old_intervals(i)
        if not free_regs:
            spill_at_interval(i)
        else:
            reg = free_regs.pop()
            registers[uop] = reg
            active_uops.add(uop)

    used_spill_registers = defaultdict(set)
    def prepare_register(uop, idx):
        if uop in registers:
            return registers[uop]
        else:
            reg = [spill_reg for spill_reg in SPILL_REGISTERS if spill_reg not in
            ↪  used_spill_registers[idx]][0]
            used_spill_registers[idx].add(reg)
            add_inst(OP_LOAD, reg, SPILL_BASE, imm=spill_locations[uop])
            return reg

```

```
130         def ensure_persisted(uop, reg):
131             if uop in spill_locations:
132                 add_inst(OP_STORE, reg, SPILL_BASE, imm=spill_locations[uop])
133 
134         # Initialize spill base calculation
135         spill_start = MAX_MEMORY - SPILL_PER_CORE
136         add_inst(OP_LOAD_IMM, 1, imm=spill_start)
137         add_inst(OP_LOAD_IMM, 2, imm=SPILL_PER_CORE)
138         add_inst(OP_MUL, 3, THREAD_ID, 2)
139         add_inst(OP_ADD, SPILL_BASE, 1, 3)
140 
141         # Process UOps
142         loop_stack = []
143         for i, uop in enumerate(uops):
144             if uop.op is Ops.SINK:
145                 add_inst(OP_HALT)
146 
147             elif uop.op is Ops.CONST:
148                 rd = prepare_register(uop, i)
149                 val = struct.unpack('I', struct.pack('f', float(uop.arg)))[0] if
                    ↪  dtypes.is_float(uop.dtype) else int(uop.arg) & 0xFFFFFFFF
150                 add_inst(OP_LOAD_IMM, rd, imm=val » 16)
151                 add_inst(OP_LOAD_IMM, SHIFT_REG, imm=16)
152                 add_inst(OP_SHL, rd, rd, SHIFT_REG)
153                 add_inst(OP_LOAD_IMM, TEMP_REG, imm=val & 0xFFFF)
154                 add_inst(OP_OR, rd, rd, TEMP_REG)
155                 ensure_persisted(uop, rd)
156 
157             elif uop.op is Ops.DEFINE_GLOBAL:
158                 rd = prepare_register(uop, i)
159                 add_inst(OP_PLACEHOLDER_BUFFER, rd, 0, uop.arg)
160                 ensure_persisted(uop, rd)
161 
162             elif uop.op is Ops.SPECIAL:
163                 rd = prepare_register(uop, i)
164                 add_inst(OP_MOV, rd, THREAD_ID)
165                 ensure_persisted(uop, rd)
166 
167             elif uop.op in GroupOp.ALU:
168                 rd = prepare_register(uop, i)
169                 rs1 = prepare_register(uop.src[0], i)
170                 rs2 = prepare_register(uop.src[1], i) if len(uop.src) > 1 else 0
171                 add_inst(get_op(uop), rd, rs1, rs2)
172                 ensure_persisted(uop, rd)
173 
174             elif uop.op is Ops.INDEX:
175                 rd = prepare_register(uop, i)
176                 base = prepare_register(uop.src[0], i)
```

```
177                 if len(uop.src) > 1:
178                     add_inst(OP_ADD, rd, base, prepare_register(uop.src[1], i))
179                 else:
180                     add_inst(OP_MOV, rd, base)
181                 ensure_persisted(uop, rd)
182 
183             elif uop.op is Ops.LOAD:
184                 rd = prepare_register(uop, i)
185                 add_inst(OP_LOAD, rd, prepare_register(uop.src[0], i))
186                 ensure_persisted(uop, rd)
187 
188 
189             elif uop.op is Ops.STORE:
190                 add_inst(OP_STORE, prepare_register(uop.src[1], i),
                    ↪  prepare_register(uop.src[0], i))
191 
192             elif uop.op is Ops.BARRIER:
193                 add_inst(OP_BARRIER)
194 
195             elif uop.op is Ops.RANGE:
196                 counter_reg = prepare_register(uop, i)
197                 loop_start_label = f"{i}"
198                 loop_end_label = f"{i+0x7FFF}"
199                 add_inst(OP_MOV, counter_reg, prepare_register(uop.src[0], i))
200                 ensure_persisted(uop, counter_reg)
201                 insts.append(loop_start_label)
202                 add_inst(OP_CMPLT, TEMP_REG, counter_reg, prepare_register(uop.src[1], i))
203                 add_inst(OP_JZ, TEMP_REG, imm=int(loop_end_label))
204                 loop_stack.append((uop, loop_start_label, loop_end_label))
205 
206             elif uop.op is Ops.ENDRANGE:
207                 counter_uop, loop_start_label, loop_end_label = loop_stack.pop()
208                 counter_reg = prepare_register(counter_uop, i)
209                 add_inst(OP_LOAD_IMM, TEMP_REG, imm=1)
210                 add_inst(OP_ADD, counter_reg, counter_reg, TEMP_REG)
211                 ensure_persisted(counter_uop, counter_reg)
212                 add_inst(OP_JMP, imm=int(loop_start_label))
213                 insts.append(loop_end_label)
214 
215         if not insts or (insts[-1] >> 26) != OP_HALT:
216             add_inst(OP_HALT)
217 
218 
219         # Add nops
220         i = 0
221         while i < len(insts):
222             nops_needed = 5 if type(insts[i]) != str else 0
223             insts[i+1:i+1] = [encode(OP_NOP) for _ in range(nops_needed)]
```

```
            i += nops_needed+1

        # Patch labels
        labels = {}
        i = 0
        while i < len(insts):
            if type(insts[i]) == str:
                label = int(insts[i])
                labels[label] = i
                del insts[i]
            else:
                i += 1
        i = 0
        while i < len(insts):
            if insts[i] >> 26 in J_OPS:
                target_label = insts[i] & 0xFFFF
                target_addr = labels[target_label]
                offset = (65536 + target_addr - i) % 65536
                insts[i] = encode(insts[i] >> 26, (insts[i] >> 21) & 0x1F, imm=offset)
            i += 1

        # Create buffer placeholder metadata
        placeholder_buffers = [(inst_idx, (inst >> 11) & 0x1F, (inst >> 21) & 0x1F) for
        ↪  inst_idx, inst in enumerate(insts) if inst >> 26 == OP_PLACEHOLDER_BUFFER]

        # Build binary
        binary = struct.pack('<II', 0xDEADBEEF, len(placeholder_buffers))
        for inst_idx, buf_idx, reg in placeholder_buffers:
            binary += struct.pack('<III', inst_idx, buf_idx, reg)
        for inst in insts:
            binary += struct.pack('<I', inst)

        return binary

    @staticmethod
    def decode_and_display_instructions(compiled_bytes: bytes, patched=True) -> str:
        """
        Decode compiled kernel and return a nicely formatted instruction listing for
        ↪  debugging

        Args:
            compiled_bytes: The compiled kernel bytes from the compiler

        Returns:
           A formatted string showing all instructions with addresses, opcodes, and operands
        """

```

```
269         # Opcode definitions (same as in compile method)
270         OPCODES = {
271             0x01: "ADD", 0x02: "SUB", 0x03: "MUL", 0x04: "DIV", 0x05: "MOD",
272             0x06: "SHL", 0x07: "SHR", 0x08: "AND", 0x09: "OR", 0x0A: "XOR",
273             0x0B: "NEG", 0x0C: "CMPLT", 0x0D: "CMPNE", 0x0E: "MAX",
274             0x10: "MOV", 0x11: "LOAD_IMM",
275 
276             # Floating point operations
277             0x12: "FADD", 0x13: "FSUB", 0x14: "FMUL", 0x15: "FDIV",
278             0x16: "FSQRT", 0x17: "FRECIP", 0x18: "FEXP2", 0x19: "FLOG2",
279             0x1A: "FMAX", 0x1B: "FNEG", 0x1C: "FNE", 0x1D: "FLT",
280             0x1E: "FTOI", 0x1F: "FTOUI", 0x22: "ITOF", 0x23: "UITOF",
281 
282             0x20: "LOAD", 0x21: "STORE",
283             0x30: "JMP", 0x31: "JZ", 0x32: "JNZ", 0x33: "JLT", 0x34: "JGE",
284             0x3E: "BARRIER", 0x3F: "NOP", 0x3D: "HALT",
285             0x00: "PLACEHOLDER"
286         }
287 
288         # Instructions that use I-type format (immediate operand)
289         I_TYPE_OPS = {0x11, 0x20, 0x21}  # LOAD_IMM, LOAD, STORE
290 
291         # Instructions that use J-type format (jump target)
292         J_TYPE_OPS = {0x30, 0x31, 0x32, 0x33, 0x34}  # JMP, JZ, JNZ, JLT, JGE
293 
294         def decode_instruction(instruction: int) -> tuple[str, str, str]:
295             """Decode a 32-bit instruction and return (opcode_name, operands, comments)"""
296             opcode = (instruction >> 26) & 0x3F
297             opcode_name = OPCODES.get(opcode, f"UNK_{opcode:02X}")
298 
299             if opcode in J_TYPE_OPS:
300                 # J-type: opcode(6) | target(26)
301                 target = instruction & 0xFFFF
302                 operands = f"0x{target:06X}"
303                 comments = f"target={target}"
304 
305             elif opcode in I_TYPE_OPS:
306                 # I-type: opcode(6) | rd(5) | rs1(5) | imm(16)
307                 rd = (instruction >> 21) & 0x1F
308                 rs1 = (instruction >> 16) & 0x1F
309                 imm = instruction & 0xFFFF
310 
311                 # Sign extend 16-bit immediate
312                 if imm & 0x8000:
313                     imm_signed = imm - 0x10000
314                 else:
315                     imm_signed = imm
316 
```

```
            operands = f"r{rd}, r{rs1}, #{imm_signed}"
            comments = f"rd=r{rd}, rs1=r{rs1}, imm={imm_signed} (0x{imm:04X})"

        else:
            # R-type: opcode(6) | rd(5) | rs1(5) | rs2(5) | unused(11)
            rd = (instruction >> 21) & 0x1F
            rs1 = (instruction >> 16) & 0x1F
            rs2 = (instruction >> 11) & 0x1F

            if opcode == 0x3F:  # NOP
                operands = ""
                comments = "no operation"
            elif opcode == 0x3D:  # HALT
                operands = ""
                comments = "halt execution"
            elif opcode in {0x0B, 0x1B}:  # NEG, FNEG (unary operations)
                operands = f"r{rd}, r{rs1}"
                comments = f"rd=r{rd}, rs1=r{rs1}"
            else:
                operands = f"r{rd}, r{rs1}, r{rs2}"
                comments = f"rd=r{rd}, rs1=r{rs1}, rs2=r{rs2}"

        return opcode_name, operands, comments

    # Parse the compiled bytes
    offset = 0
    placeholders = []

    if not patched:
        # Read header
        magic = struct.unpack('<I', compiled_bytes[offset:offset+4])[0]
        offset += 4

        if magic != 0xDEADBEEF:
            return f"Error: Invalid magic number 0x{magic:08X}, expected 0xDEADBEEF"

        num_placeholders = struct.unpack('<I', compiled_bytes[offset:offset+4])[0]
        offset += 4
        # Read placeholders
        for i in range(num_placeholders):
            inst_idx, buf_idx, reg = struct.unpack('<III',
            ↪  compiled_bytes[offset:offset+12])
            placeholders.append((inst_idx, buf_idx, reg))
            offset += 12

    # Read instructions
    instructions = []
    while offset < len(compiled_bytes):
```

```
364             inst = struct.unpack('<I', compiled_bytes[offset:offset+4])[0]
365             instructions.append(inst)
366             offset += 4
367 
368         # Format the output
369         output = []
370         output.append("=" * 80)
371         output.append("RIVYERA INSTRUCTION LISTING")
372         output.append("=" * 80)
373         output.append("")
374 
375         if placeholders:
376             output.append("BUFFER PLACEHOLDERS:")
377             for inst_idx, buf_idx, reg in placeholders:
378                 output.append(f"  Instruction {inst_idx:3d}: Buffer {buf_idx} -> Register
                    ↪  r{reg}")
379             output.append("")
380 
381         output.append("INSTRUCTIONS:")
382         output.append("Addr   Hex        Opcode     Operands           ; Comments")
383         output.append("-" * 80)
384 
385         for i, instruction in enumerate(instructions):
386             opcode_name, operands, comments = decode_instruction(instruction)
387 
388             addr_str = f"{i:4d}:"
389             hex_str = f"0x{instruction:08X}"
390             opcode_str = f"{opcode_name:<10}"
391             operands_str = f"{operands:<18}"
392 
393             # Mark placeholders
394             is_placeholder = any(inst_idx == i for inst_idx, _, _ in placeholders)
395             placeholder_mark = " *" if is_placeholder else "  "
396 
397             line = f"{addr_str} {hex_str} {opcode_str} {operands_str} ;
                ↪  {comments}{placeholder_mark}"
398             output.append(line)
399 
400         output.append("-" * 80)
401         output.append(f"Total instructions: {len(instructions)}")
402 
403         if placeholders:
404             output.append("* = Placeholder instruction (will be patched at runtime)")
405 
406         output.append("=" * 80)
407 
408         return "\n".join(output)
```

# C Appendix C: Functional Correctness Test

```python
import os
os.environ["DEBUG"] = "6"  # Enables verbose logging to see UOp tree and kernels
os.environ["RIVYERA"] = "1"   # Forces Rivyera device usage
os.environ["RIVYERA_SIM"] = "1" # Enable FPGA simulation
os.environ["DISPLAY"] = ":1"

import unittest
import numpy as np
from tinygrad import Tensor, Device, dtypes
from tinygrad.helpers import getenv, CI
from tinygrad.device import is_dtype_supported
from tinygrad.ops import Ops, UOp
import time

@unittest.skipUnless(Device.DEFAULT == "RIVYERA" or "RIVYERA" in Device._devices, "RIVYERA device required")
class TestRivyeraOps(unittest.TestCase):
    @classmethod
    def setUpClass(cls):
        """Set up the test class with Rivyera device"""
        try:
            cls.device = Device["RIVYERA:0"]
            # Test basic device functionality
            cls.device.synchronize()
            print(f"Using Rivyera device: {cls.device}")
        except Exception as e:
            raise unittest.SkipTest(f"Rivyera device not available: {e}")

    def setUp(self):
        """Reset device state before each test"""
        self.device.synchronize()

    def test_matmul_1(self):
        print("\n=== test_matmul_1 ===")
        # Create test matrices
        a_data = np.ones((4, 4), dtype=np.int32)
        b_data = np.arange(1, 17, dtype=np.int32).reshape(4, 4)
        expected_result = a_data * b_data
        print(f"Matrix A:\n{a_data}")
        print(f"Matrix B:\n{b_data}")
        print(f"Expected A * B:\n{expected_result}")

        # Create tensors on Rivyera device
        a = Tensor(a_data, device="RIVYERA:0", dtype=dtypes.int32)
        b = Tensor(b_data, device="RIVYERA:0", dtype=dtypes.int32)
```

```
45
46          # Perform elementwise multiplication
47          c = a * b
48
49          # Realize the computation (this triggers compilation and execution)
50          result = c.realize()
51
52          # Verify result
53          result_np = result.numpy()
54          print(f"Actual result:\n{result_np}")
55
56          # Check that results match expected values
57          np.testing.assert_allclose(result_np, expected_result, rtol=1e-5, atol=1e-6,
58                                     err_msg="Elemwise Multiplication result doesn't match
                                       ↪  expected")
59
60          print(" Matmul test 1 passed!")
61
62      def test_matmul_2(self):
63          print("\n=== test_matmul_2 ===")
64
65          # Create test matrices
66          a_data = np.eye(2, dtype=np.int32)
67          b_data = np.arange(1, 5, dtype=np.int32).reshape(2, 2)
68          expected_result = a_data @ b_data
69          print(f"Matrix A:\n{a_data}")
70          print(f"Matrix B:\n{b_data}")
71          print(f"Expected A @ B:\n{expected_result}")
72
73          # Create tensors on Rivyera device
74          a = Tensor(a_data, device="RIVYERA:0", dtype=dtypes.int32)
75          b = Tensor(b_data, device="RIVYERA:0", dtype=dtypes.int32)
76
77          # Perform elementwise multiplication
78          c = a @ b
79
80          # Realize the computation (this triggers compilation and execution)
81          result = c.realize()
82
83          # Verify result
84          result_np = result.numpy()
85          print(f"Actual result:\n{result_np}")
86
87          # Check that results match expected values
88          np.testing.assert_allclose(result_np, expected_result, rtol=1e-5, atol=1e-6,
89                                     err_msg="Matrix Multiplication result doesn't match expected")
90
91          print(" Matmul test 2 passed!")
```

```

    def tearDown(self):
        """Clean up after each test"""
        self.device.synchronize()

    @classmethod
    def tearDownClass(cls):
        """Clean up the test class"""
        if hasattr(cls, 'device'):
            cls.device.synchronize()


if __name__ == '__main__':
    unittest.main()
```

# D Appendix D: Timing Report

```
--------------------------------------------------------------------------------
Release 14.7 Trace  (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.

/opt/Xilinx/14.7/ISE_DS/ISE/bin/lin64/unwrapped/trce -intstyle ise -v 3 -s 3 -n
3 -fastpaths -xml rivyera_accelerator_top.twx rivyera_accelerator_top.ncd -o
rivyera_accelerator_top.twr rivyera_accelerator_top.pcf

Design file:              rivyera_accelerator_top.ncd
Physical constraint file: rivyera_accelerator_top.pcf
Device,package,speed:     xc6slx150,fgg676,C,-3 (PRODUCTION 1.23 2013-10-13)
Report level:             verbose report

Environment Variable      Effect
--------------------      ------
NONE                      No environment variables were set
--------------------------------------------------------------------------------

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
   option. All paths that are not constrained will be reported in the
   unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.

================================================================================
```

```
Timing constraint: TS_CPI_CLK = PERIOD TIMEGRP "CPI_CLK" 10 ns HIGH 50%;
For more information, see Period Analysis in the Timing Closure User Guide (UG612).

 0 paths analyzed, 0 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 component switching limit errors)
 Minimum period is   3.334ns.
--------------------------------------------------------------------------------

Component Switching Limit Checks: TS_CPI_CLK = PERIOD TIMEGRP "CPI_CLK" 10 ns HIGH 50%;
--------------------------------------------------------------------------------
Slack: 6.666ns (period - (min low pulse limit / (low pulse / period)))
  Period: 10.000ns
  Low pulse: 5.000ns
  Low pulse limit: 1.667ns (Tdcmpw_CLKIN_100_150)
  Physical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y2.CLKIN2
  Clock network: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------
Slack: 6.666ns (period - (min high pulse limit / (high pulse / period)))
  Period: 10.000ns
  High pulse: 5.000ns
  High pulse limit: 1.667ns (Tdcmpw_CLKIN_100_150)
  Physical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y2.CLKIN2
  Clock network: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------
Slack: 8.148ns (period - min period limit)
  Period: 10.000ns
  Min period limit: 1.852ns (539.957MHz) (Tpllper_CLKIN(Finmax))
  Physical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y2.CLKIN2
  Clock network: SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TS_CNI_CLK = PERIOD TIMEGRP "CNI_CLK" 10 ns HIGH 50%;
For more information, see Period Analysis in the Timing Closure User Guide (UG612).

 0 paths analyzed, 0 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 component switching limit errors)
 Minimum period is   3.334ns.
--------------------------------------------------------------------------------

Component Switching Limit Checks: TS_CNI_CLK = PERIOD TIMEGRP "CNI_CLK" 10 ns HIGH 50%;
--------------------------------------------------------------------------------
```

```
Slack: 6.666ns (period - (min low pulse limit / (low pulse / period)))
  Period: 10.000ns
  Low pulse: 5.000ns
  Low pulse limit: 1.667ns (Tdcmpw_CLKIN_100_150)
  Physical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y3.CLKIN1
  Clock network: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------
Slack: 6.666ns (period - (min high pulse limit / (high pulse / period)))
  Period: 10.000ns
  High pulse: 5.000ns
  High pulse limit: 1.667ns (Tdcmpw_CLKIN_100_150)
  Physical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y3.CLKIN1
  Clock network: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------
Slack: 8.148ns (period - min period limit)
  Period: 10.000ns
  Min period limit: 1.852ns (539.957MHz) (Tpllper_CLKIN(Finmax))
  Physical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Logical resource: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV/CLKIN1
  Location pin: PLL_ADV_X0Y3.CLKIN1
  Clock network: SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout1 = PERIOD
TIMEGRP         "SciEngines_API_Core_api_clk_mgmt_up_clkout1" TS_CPI_CLK PHASE
       -0.416666667 ns HIGH 50%;
For more information, see Period Analysis in the Timing Closure User Guide (UG612).

 87137019 paths analyzed, 37060 endpoints analyzed, 159 failing endpoints
 159 timing errors detected. (159 setup errors, 0 hold errors, 0 component switching limit
  ↪ errors)
 Minimum period is  15.943ns.
--------------------------------------------------------------------------------

Paths for end point
  ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
  ↪ (SLICE_X96Y92.DX), 5671927 paths
--------------------------------------------------------------------------------
Slack (setup path):     -5.943ns (requirement - (data path - clock path skew + uncertainty))
  Source:
   ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
```

```
119 Destination:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
    ↪ (FF)
120 Requirement:          10.000ns
121 Data Path Delay:      15.834ns (Levels of Logic = 6)(Component delays alone exceeds
    ↪ constraint)
122 Clock Path Skew:      -0.012ns (0.240 - 0.252)
123 Source Clock:         api_clk rising at -0.416ns
124 Destination Clock:    api_clk rising at 9.584ns
125 Clock Uncertainty:    0.097ns
126
127 Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
128   Total System Jitter (TSJ):  0.070ns
129   Discrete Jitter (DJ):       0.181ns
130   Phase Error (PE):           0.000ns
131
132 Maximum Data Path at Slow Process Corner:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
133   Location             Delay type         Delay(ns)  Physical Resource
134                                                        Logical Resource(s)
135   -------------------------------------------------  -------------------
136   SLICE_X117Y86.AQ     Tcko                  0.391
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
137                                                    user_core/multi_core_system/gen_cores[0
                                                           ↪ ].core_inst/id_stage/rs2_reg_1
138   SLICE_X109Y76.C6     net (fanout=219)      1.377
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
139   SLICE_X109Y76.C      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
140                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_913
141   SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
142   SLICE_X106Y85.A      Tilo                  0.205
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
143                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_44
144   SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
145   SLICE_X109Y86.D      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
```

```
146                                                 user_core/multi_core_system/gen_cores[0].
                                                        ↪ core_inst/ex_stage/Mmux_alu_b51
147     DSP48_X2Y20.B13      net (fanout=11)       1.114
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
148     DSP48_X2Y20.P17      Tdspdo_B_P            3.748
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
149                                       user_core/multi_core_system/gen_cores[0].core_ins
                                                        ↪ t/ex_stage/alu_inst/Mmult_n0100
150     DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
151     DSP48_X2Y21.PCOUT0   Tdspdo_C_PCOUT        2.689
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
152                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                        ↪ /ex_stage/alu_inst/Mmult_n01001
153     DSP48_X2Y22.PCIN0    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_0
154     DSP48_X2Y22.P2       Tdspdo_PCIN_P         2.264
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
155                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                        ↪ /ex_stage/alu_inst/Mmult_n01002
156     SLICE_X96Y92.DX      net (fanout=2)        0.922
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<19>
157     SLICE_X96Y92.CLK     Tdick                 0.136
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
158                                       user_core/multi_core_system/gen_cores[0].core_ins
                                                        ↪ t/ex_stage/mem_addr_reg_19_BRB3
159     ----------------------------------------------  ---------------------------
160     Total                                     15.834ns (9.951ns logic, 5.883ns route)
161                                                      (62.8% logic, 37.2% route)
162
163 --------------------------------------------------------------------------------
164 Slack (setup path):     -5.943ns (requirement - (data path - clock path skew + uncertainty))
165   Source:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
166   Destination:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
      ↪ (FF)
167   Requirement:          10.000ns
168   Data Path Delay:      15.834ns (Levels of Logic = 6)(Component delays alone exceeds
      ↪ constraint)
169   Clock Path Skew:      -0.012ns (0.240 - 0.252)
170   Source Clock:         api_clk rising at -0.416ns
171   Destination Clock:    api_clk rising at 9.584ns
172   Clock Uncertainty:    0.097ns
173
174   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
175     Total System Jitter (TSJ):  0.070ns
```

```
176   Discrete Jitter (DJ):       0.181ns
177   Phase Error (PE):           0.000ns
178
179 Maximum Data Path at Slow Process Corner:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
180   Location             Delay type         Delay(ns)  Physical Resource
181                                                        Logical Resource(s)
182   -------------------------------------------------  -------------------
183   SLICE_X117Y86.AQ     Tcko                  0.391
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
184                                                    user_core/multi_core_system/gen_cores[0
                                                           ↪ ].core_inst/id_stage/rs2_reg_1
185   SLICE_X109Y76.C6     net (fanout=219)      1.377
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
186   SLICE_X109Y76.C      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
187                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_913
188   SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
189   SLICE_X106Y85.A      Tilo                  0.205
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
190                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_44
191   SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
192   SLICE_X109Y86.D      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
193                                                  user_core/multi_core_system/gen_cores[0].
                                                           ↪ core_inst/ex_stage/Mmux_alu_b51
194   DSP48_X2Y20.B13      net (fanout=11)       1.114
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
195   DSP48_X2Y20.P17      Tdspdo_B_P            3.748
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
196                                      user_core/multi_core_system/gen_cores[0].core_ins
                                                           ↪ t/ex_stage/alu_inst/Mmult_n0100
197   DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
198   DSP48_X2Y21.PCOUT9   Tdspdo_C_PCOUT        2.689
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
199                                    user_core/multi_core_system/gen_cores[0].core_inst
                                                           ↪ /ex_stage/alu_inst/Mmult_n01001
```

```
    DSP48_X2Y22.PCIN9    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor⌋
    ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_9
    DSP48_X2Y22.P2       Tdspdo_PCIN_P         2.264
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
                                       user_core/multi_core_system/gen_cores[0].core_inst⌋
                                                    ↪ /ex_stage/alu_inst/Mmult_n01002
    SLICE_X96Y92.DX      net (fanout=2)        0.922
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<19>
    SLICE_X96Y92.CLK     Tdick                 0.136
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
                                        user_core/multi_core_system/gen_cores[0].core_ins⌋
                                                    ↪ t/ex_stage/mem_addr_reg_19_BRB3
    ---------------------------------------------  --------------------------
    Total                                      15.834ns (9.951ns logic, 5.883ns route)
                                                    (62.8% logic, 37.2% route)

--------------------------------------------------------------------------------
Slack (setup path):     -5.943ns (requirement - (data path - clock path skew + uncertainty))
  Source:
  ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
  Destination:
  ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
  ↪ (FF)
  Requirement:          10.000ns
  Data Path Delay:      15.834ns (Levels of Logic = 6)(Component delays alone exceeds
  ↪ constraint)
  Clock Path Skew:      -0.012ns (0.240 - 0.252)
  Source Clock:         api_clk rising at -0.416ns
  Destination Clock:    api_clk rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
  ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
  ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X117Y86.AQ     Tcko                  0.391
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
                                              user_core/multi_core_system/gen_cores[0⌋
                                                    ↪ ].core_inst/id_stage/rs2_reg_1
```

```
232  SLICE_X109Y76.C6     net (fanout=219)      1.377
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
233  SLICE_X109Y76.C      Tilo                  0.259
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
234                                                user_core/multi_core_system/gen_cores
                                                   ↪ [0].core_inst/reg_file/Mmux_rf
                                                   ↪ _rs2_addr[4]_registers[31][31]
                                                   ↪ _wide_mux_2_OUT_913
235  SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
     ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
236  SLICE_X106Y85.A      Tilo                  0.205
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
237                                                user_core/multi_core_system/gen_cores
                                                   ↪ [0].core_inst/reg_file/Mmux_rf
                                                   ↪ _rs2_addr[4]_registers[31][31]
                                                   ↪ _wide_mux_2_OUT_44
238  SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
     ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
239  SLICE_X109Y86.D      Tilo                  0.259
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
240                                              user_core/multi_core_system/gen_cores[0].
                                                   ↪ core_inst/ex_stage/Mmux_alu_b51
241  DSP48_X2Y20.B13      net (fanout=11)       1.114
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
242  DSP48_X2Y20.P17      Tdspdo_B_P            3.748
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
243                                     user_core/multi_core_system/gen_cores[0].core_ins
                                                   ↪ t/ex_stage/alu_inst/Mmult_n0100
244  DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
     ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
245  DSP48_X2Y21.PCOUT1   Tdspdo_C_PCOUT        2.689
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
246                                    user_core/multi_core_system/gen_cores[0].core_inst
                                                   ↪ /ex_stage/alu_inst/Mmult_n01001
247  DSP48_X2Y22.PCIN1    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
     ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_1
248  DSP48_X2Y22.P2       Tdspdo_PCIN_P         2.264
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
249                                    user_core/multi_core_system/gen_cores[0].core_inst
                                                   ↪ /ex_stage/alu_inst/Mmult_n01002
250  SLICE_X96Y92.DX      net (fanout=2)        0.922
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<19>
251  SLICE_X96Y92.CLK     Tdick                 0.136
     ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_19_BRB3
252                                     user_core/multi_core_system/gen_cores[0].core_ins
                                                   ↪ t/ex_stage/mem_addr_reg_19_BRB3
253  ----------------------------------------------  ---------------------------
```

```
254    Total                                     15.834ns (9.951ns logic, 5.883ns route)
255                                                     (62.8% logic, 37.2% route)
256
257 --------------------------------------------------------------------------------
258
259 Paths for end point
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
    ↪ (SLICE_X95Y89.BX), 5671927 paths
260 --------------------------------------------------------------------------------
261 Slack (setup path):     -5.856ns (requirement - (data path - clock path skew + uncertainty))
262   Source:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
263   Destination:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
      ↪ (FF)
264   Requirement:          10.000ns
265   Data Path Delay:      15.740ns (Levels of Logic = 6)
266   Clock Path Skew:      -0.019ns (0.233 - 0.252)
267   Source Clock:         api_clk rising at -0.416ns
268   Destination Clock:    api_clk rising at 9.584ns
269   Clock Uncertainty:    0.097ns
270
271   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
272     Total System Jitter (TSJ):  0.070ns
273     Discrete Jitter (DJ):       0.181ns
274     Phase Error (PE):           0.000ns
275
276   Maximum Data Path at Slow Process Corner:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
277     Location             Delay type         Delay(ns)  Physical Resource
278                                                        Logical Resource(s)
279     -------------------------------------------------  -------------------
280     SLICE_X117Y86.AQ     Tcko                  0.391
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
281                                                    user_core/multi_core_system/gen_cores[0
                                                           ↪ ].core_inst/id_stage/rs2_reg_1
282     SLICE_X109Y76.C6     net (fanout=219)      1.377
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
283     SLICE_X109Y76.C      Tilo                  0.259
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
284                                                      user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_913
285     SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
```

```
286     SLICE_X106Y85.A      Tilo                  0.205
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
287                                                   user_core/multi_core_system/gen_cores
                                                         ↪ [0].core_inst/reg_file/Mmux_rf
                                                         ↪ _rs2_addr[4]_registers[31][31]
                                                         ↪ _wide_mux_2_OUT_44
288     SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
289     SLICE_X109Y86.D      Tilo                  0.259
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
290                                                 user_core/multi_core_system/gen_cores[0].
                                                         ↪ core_inst/ex_stage/Mmux_alu_b51
291     DSP48_X2Y20.B13      net (fanout=11)       1.114
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
292     DSP48_X2Y20.P17      Tdspdo_B_P            3.748
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
293                                       user_core/multi_core_system/gen_cores[0].core_ins
                                                         ↪ t/ex_stage/alu_inst/Mmult_n0100
294     DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
295     DSP48_X2Y21.PCOUT0   Tdspdo_C_PCOUT        2.689
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
296                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                         ↪ /ex_stage/alu_inst/Mmult_n01001
297     DSP48_X2Y22.PCIN0    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_0
298     DSP48_X2Y22.P1       Tdspdo_PCIN_P         2.264
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
299                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                         ↪ /ex_stage/alu_inst/Mmult_n01002
300     SLICE_X95Y89.BX      net (fanout=2)        0.901
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<18>
301     SLICE_X95Y89.CLK     Tdick                 0.063
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
302                                       user_core/multi_core_system/gen_cores[0].core_ins
                                                         ↪ t/ex_stage/mem_addr_reg_18_BRB3
303     -------------------------------------------------  ---------------------------
304     Total                                     15.740ns (9.878ns logic, 5.862ns route)
305                                                        (62.8% logic, 37.2% route)
306
307 --------------------------------------------------------------------------------
308 Slack (setup path):     -5.856ns (requirement - (data path - clock path skew + uncertainty))
309   Source:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
310   Destination:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
      ↪ (FF)
```

```
Requirement:          10.000ns
Data Path Delay:      15.740ns (Levels of Logic = 6)
Clock Path Skew:      -0.019ns (0.233 - 0.252)
Source Clock:         api_clk rising at -0.416ns
Destination Clock:    api_clk rising at 9.584ns
Clock Uncertainty:    0.097ns

Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.070ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.000ns

Maximum Data Path at Slow Process Corner:
  user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
  user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  SLICE_X117Y86.AQ     Tcko                  0.391
  user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
                                                     user_core/multi_core_system/gen_cores[0
                                                       ].core_inst/id_stage/rs2_reg_1
  SLICE_X109Y76.C6     net (fanout=219)      1.377
  user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
  SLICE_X109Y76.C      Tilo                  0.259
  user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
                                                     user_core/multi_core_system/gen_cores
                                                       [0].core_inst/reg_file/Mmux_rf
                                                       _rs2_addr[4]_registers[31][31]
                                                       _wide_mux_2_OUT_913
  SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
  es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
  SLICE_X106Y85.A      Tilo                  0.205
  user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
                                                     user_core/multi_core_system/gen_cores
                                                       [0].core_inst/reg_file/Mmux_rf
                                                       _rs2_addr[4]_registers[31][31]
                                                       _wide_mux_2_OUT_44
  SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
  es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
  SLICE_X109Y86.D      Tilo                  0.259
  user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
                                                     user_core/multi_core_system/gen_cores[0].
                                                       core_inst/ex_stage/Mmux_alu_b51
  DSP48_X2Y20.B13      net (fanout=11)       1.114
  user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
```

```
339     DSP48_X2Y20.P17      Tdspdo_B_P            3.748
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
340                                          user_core/multi_core_system/gen_cores[0].core_ins⌋
                                                     ↪ t/ex_stage/alu_inst/Mmult_n0100
341     DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor⌋
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
342     DSP48_X2Y21.PCOUT9   Tdspdo_C_PCOUT        2.689
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
343                                        user_core/multi_core_system/gen_cores[0].core_inst⌋
                                                     ↪ /ex_stage/alu_inst/Mmult_n01001
344     DSP48_X2Y22.PCIN9    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor⌋
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_9
345     DSP48_X2Y22.P1       Tdspdo_PCIN_P         2.264
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
346                                        user_core/multi_core_system/gen_cores[0].core_inst⌋
                                                     ↪ /ex_stage/alu_inst/Mmult_n01002
347     SLICE_X95Y89.BX      net (fanout=2)        0.901
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<18>
348     SLICE_X95Y89.CLK     Tdick                 0.063
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
349                                          user_core/multi_core_system/gen_cores[0].core_ins⌋
                                                     ↪ t/ex_stage/mem_addr_reg_18_BRB3
350     ------------------------------------------------  ---------------------------
351     Total                                      15.740ns (9.878ns logic, 5.862ns route)
352                                                      (62.8% logic, 37.2% route)
353
354 --------------------------------------------------------------------------------
355 Slack (setup path):     -5.856ns (requirement - (data path - clock path skew + uncertainty))
356   Source:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
357   Destination:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
      ↪ (FF)
358   Requirement:          10.000ns
359   Data Path Delay:      15.740ns (Levels of Logic = 6)
360   Clock Path Skew:      -0.019ns (0.233 - 0.252)
361   Source Clock:         api_clk rising at -0.416ns
362   Destination Clock:    api_clk rising at 9.584ns
363   Clock Uncertainty:    0.097ns
364
365   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
366     Total System Jitter (TSJ):  0.070ns
367     Discrete Jitter (DJ):       0.181ns
368     Phase Error (PE):           0.000ns
369
```

```
370 Maximum Data Path at Slow Process Corner:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
371   Location             Delay type         Delay(ns)  Physical Resource
372                                                      Logical Resource(s)
373   -------------------------------------------------  -------------------
374   SLICE_X117Y86.AQ     Tcko                  0.391
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
375                                                    user_core/multi_core_system/gen_cores[0
                                                           ↪ ].core_inst/id_stage/rs2_reg_1
376   SLICE_X109Y76.C6     net (fanout=219)      1.377
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
377   SLICE_X109Y76.C      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
378                                                      user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_913
379   SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
380   SLICE_X106Y85.A      Tilo                  0.205
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
381                                                      user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_44
382   SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
383   SLICE_X109Y86.D      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
384                                                    user_core/multi_core_system/gen_cores[0].
                                                           ↪ core_inst/ex_stage/Mmux_alu_b51
385   DSP48_X2Y20.B13      net (fanout=11)       1.114
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
386   DSP48_X2Y20.P17      Tdspdo_B_P            3.748
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
387                                          user_core/multi_core_system/gen_cores[0].core_ins
                                                           ↪ t/ex_stage/alu_inst/Mmult_n0100
388   DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
389   DSP48_X2Y21.PCOUT1   Tdspdo_C_PCOUT        2.689
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
390                                        user_core/multi_core_system/gen_cores[0].core_inst
                                                           ↪ /ex_stage/alu_inst/Mmult_n01001
391   DSP48_X2Y22.PCIN1    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_1
```

```
392     DSP48_X2Y22.P1       Tdspdo_PCIN_P         2.264
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
393                                       user_core/multi_core_system/gen_cores[0].core_inst⌋
                                                  ↪ /ex_stage/alu_inst/Mmult_n01002
394     SLICE_X95Y89.BX      net (fanout=2)        0.901
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<18>
395     SLICE_X95Y89.CLK     Tdick                 0.063
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_18_BRB3
396                                      user_core/multi_core_system/gen_cores[0].core_ins⌋
                                                  ↪ t/ex_stage/mem_addr_reg_18_BRB3
397     -------------------------------------------------  ---------------------------
398     Total                                      15.740ns (9.878ns logic, 5.862ns route)
399                                                         (62.8% logic, 37.2% route)
400
401 --------------------------------------------------------------------------------
402
403 Paths for end point
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
    ↪ (SLICE_X97Y88.DX), 5671927 paths
404 --------------------------------------------------------------------------------
405 Slack (setup path):     -5.811ns (requirement - (data path - clock path skew + uncertainty))
406   Source:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
407   Destination:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
      ↪ (FF)
408   Requirement:          10.000ns
409   Data Path Delay:      15.693ns (Levels of Logic = 6)
410   Clock Path Skew:      -0.021ns (0.231 - 0.252)
411   Source Clock:         api_clk rising at -0.416ns
412   Destination Clock:    api_clk rising at 9.584ns
413   Clock Uncertainty:    0.097ns
414
415   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
416     Total System Jitter (TSJ):  0.070ns
417     Discrete Jitter (DJ):       0.181ns
418     Phase Error (PE):           0.000ns
419
420   Maximum Data Path at Slow Process Corner:
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
421     Location             Delay type         Delay(ns)  Physical Resource
422                                                        Logical Resource(s)
423     -------------------------------------------------  -------------------
424     SLICE_X117Y86.AQ     Tcko                  0.391
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
```

```
425                                                  user_core/multi_core_system/gen_cores[0
                                                         ↪ ].core_inst/id_stage/rs2_reg_1
426     SLICE_X109Y76.C6     net (fanout=219)      1.377
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
427     SLICE_X109Y76.C      Tilo                  0.259
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
428                                                  user_core/multi_core_system/gen_cores
                                                         ↪ [0].core_inst/reg_file/Mmux_rf
                                                         ↪ _rs2_addr[4]_registers[31][31]
                                                         ↪ _wide_mux_2_OUT_913
429     SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
430     SLICE_X106Y85.A      Tilo                  0.205
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
431                                                  user_core/multi_core_system/gen_cores
                                                         ↪ [0].core_inst/reg_file/Mmux_rf
                                                         ↪ _rs2_addr[4]_registers[31][31]
                                                         ↪ _wide_mux_2_OUT_44
432     SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
433     SLICE_X109Y86.D      Tilo                  0.259
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
434                                                user_core/multi_core_system/gen_cores[0].
                                                         ↪ core_inst/ex_stage/Mmux_alu_b51
435     DSP48_X2Y20.B13      net (fanout=11)       1.114
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
436     DSP48_X2Y20.P17      Tdspdo_B_P            3.748
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
437                                      user_core/multi_core_system/gen_cores[0].core_ins
                                                         ↪ t/ex_stage/alu_inst/Mmult_n0100
438     DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
439     DSP48_X2Y21.PCOUT0   Tdspdo_C_PCOUT        2.689
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
440                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                         ↪ /ex_stage/alu_inst/Mmult_n01001
441     DSP48_X2Y22.PCIN0    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
        ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_0
442     DSP48_X2Y22.P8       Tdspdo_PCIN_P         2.264
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
443                                     user_core/multi_core_system/gen_cores[0].core_inst
                                                         ↪ /ex_stage/alu_inst/Mmult_n01002
444     SLICE_X97Y88.DX      net (fanout=2)        0.854
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<25>
445     SLICE_X97Y88.CLK     Tdick                 0.063
        ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
```

```
                                          user_core/multi_core_system/gen_cores[0].core_ins
                                                                                    t/ex_stage/mem_addr_reg_25_BRB3
    ------------------------------------------------  -------------------------
    Total                                    15.693ns (9.878ns logic, 5.815ns route)
                                                      (62.9% logic, 37.1% route)

--------------------------------------------------------------------------------
Slack (setup path):     -5.811ns (requirement - (data path - clock path skew + uncertainty))
  Source:
    user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
  Destination:
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
    (FF)
  Requirement:          10.000ns
  Data Path Delay:      15.693ns (Levels of Logic = 6)
  Clock Path Skew:      -0.021ns (0.231 - 0.252)
  Source Clock:         api_clk rising at -0.416ns
  Destination Clock:    api_clk rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
    user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X117Y86.AQ     Tcko                  0.391
      user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
                                                 user_core/multi_core_system/gen_cores[0
                                                                                    ].core_inst/id_stage/rs2_reg_1
    SLICE_X109Y76.C6     net (fanout=219)      1.377
      user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
    SLICE_X109Y76.C      Tilo                  0.259
      user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
                                                   user_core/multi_core_system/gen_cores
                                                                                    [0].core_inst/reg_file/Mmux_rf
                                                                                    _rs2_addr[4]_registers[31][31]
                                                                                    _wide_mux_2_OUT_913
    SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
      es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
    SLICE_X106Y85.A      Tilo                  0.205
      user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
```

```
                                                    user_core/multi_core_system/gen_cores
                                                      ↪ [0].core_inst/reg_file/Mmux_rf
                                                      ↪ _rs2_addr[4]_registers[31][31]
                                                      ↪ _wide_mux_2_OUT_44
    SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
    ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
    SLICE_X109Y86.D      Tilo                  0.259
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
                                                user_core/multi_core_system/gen_cores[0].
                                                      ↪ core_inst/ex_stage/Mmux_alu_b51
    DSP48_X2Y20.B13      net (fanout=11)       1.114
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
    DSP48_X2Y20.P17      Tdspdo_B_P            3.748
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
                                          user_core/multi_core_system/gen_cores[0].core_ins
                                                      ↪ t/ex_stage/alu_inst/Mmult_n0100
    DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
    ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
    DSP48_X2Y21.PCOUT9   Tdspdo_C_PCOUT        2.689
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
                                         user_core/multi_core_system/gen_cores[0].core_inst
                                                      ↪ /ex_stage/alu_inst/Mmult_n01001
    DSP48_X2Y22.PCIN9    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
    ↪ es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_9
    DSP48_X2Y22.P8       Tdspdo_PCIN_P         2.264
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
                                         user_core/multi_core_system/gen_cores[0].core_inst
                                                      ↪ /ex_stage/alu_inst/Mmult_n01002
    SLICE_X97Y88.DX      net (fanout=2)        0.854
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<25>
    SLICE_X97Y88.CLK     Tdick                 0.063
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
                                          user_core/multi_core_system/gen_cores[0].core_ins
                                                      ↪ t/ex_stage/mem_addr_reg_25_BRB3
    -------------------------------------------------  ---------------------------
    Total                                      15.693ns (9.878ns logic, 5.815ns route)
                                                       (62.9% logic, 37.1% route)

--------------------------------------------------------------------------------
Slack (setup path):     -5.811ns (requirement - (data path - clock path skew + uncertainty))
  Source:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 (FF)
  Destination:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
    ↪ (FF)
  Requirement:          10.000ns
  Data Path Delay:      15.693ns (Levels of Logic = 6)
```

```
504 Clock Path Skew:      -0.021ns (0.231 - 0.252)
505 Source Clock:         api_clk rising at -0.416ns
506 Destination Clock:    api_clk rising at 9.584ns
507 Clock Uncertainty:    0.097ns
508
509 Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
510   Total System Jitter (TSJ):  0.070ns
511   Discrete Jitter (DJ):       0.181ns
512   Phase Error (PE):           0.000ns
513
514 Maximum Data Path at Slow Process Corner:
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg_1 to
    ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
515   Location             Delay type         Delay(ns)  Physical Resource
516                                                      Logical Resource(s)
517   -------------------------------------------------  -------------------
518   SLICE_X117Y86.AQ     Tcko                  0.391
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<0>
519                                                    user_core/multi_core_system/gen_cores[0
                                                           ↪ ].core_inst/id_stage/rs2_reg_1
520   SLICE_X109Y76.C6     net (fanout=219)      1.377
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/id_stage/rs2_reg<1>
521   SLICE_X109Y76.C      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_6<15>
522                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_913
523   SLICE_X106Y85.A5     net (fanout=1)        0.820   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_913
524   SLICE_X106Y85.A      Tilo                  0.205
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_2<15>
525                                                    user_core/multi_core_system/gen_cores
                                                           ↪ [0].core_inst/reg_file/Mmux_rf
                                                           ↪ _rs2_addr[4]_registers[31][31]
                                                           ↪ _wide_mux_2_OUT_44
526   SLICE_X109Y86.D3     net (fanout=1)        0.526   user_core/multi_core_system/gen_cor
      ↪ es[0].core_inst/reg_file/Mmux_rf_rs2_addr[4]_registers[31][31]_wide_mux_2_OUT_44
527   SLICE_X109Y86.D      Tilo                  0.259
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/reg_file/registers_17<15>
528                                                      user_core/multi_core_system/gen_cores[0].
                                                           ↪ core_inst/ex_stage/Mmux_alu_b51
529   DSP48_X2Y20.B13      net (fanout=11)       1.114
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_b<13>
530   DSP48_X2Y20.P17      Tdspdo_B_P            3.748
      ↪ user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n0100
```

```
                                        user_core/multi_core_system/gen_cores[0].core_ins
                                                                    t/ex_stage/alu_inst/Mmult_n0100
    DSP48_X2Y21.C0       net (fanout=1)        1.065   user_core/multi_core_system/gen_cor
    es[0].core_inst/ex_stage/alu_inst/Mmult_n0100_P17_to_Mmult_n01001
    DSP48_X2Y21.PCOUT1   Tdspdo_C_PCOUT        2.689
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01001
                                       user_core/multi_core_system/gen_cores[0].core_inst
                                                                    /ex_stage/alu_inst/Mmult_n01001
    DSP48_X2Y22.PCIN1    net (fanout=1)        0.059   user_core/multi_core_system/gen_cor
    es[0].core_inst/ex_stage/alu_inst/Mmult_n01001_PCOUT_to_Mmult_n01002_PCIN_1
    DSP48_X2Y22.P8       Tdspdo_PCIN_P         2.264
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/Mmult_n01002
                                       user_core/multi_core_system/gen_cores[0].core_inst
                                                                    /ex_stage/alu_inst/Mmult_n01002
    SLICE_X97Y88.DX      net (fanout=2)        0.854
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/alu_inst/n0100<25>
    SLICE_X97Y88.CLK     Tdick                 0.063
    user_core/multi_core_system/gen_cores[0].core_inst/ex_stage/mem_addr_reg_25_BRB3
                                        user_core/multi_core_system/gen_cores[0].core_ins
                                                                    t/ex_stage/mem_addr_reg_25_BRB3
    ------------------------------------------------  ---------------------------
    Total                                     15.693ns (9.878ns logic, 5.815ns route)
                                                       (62.9% logic, 37.1% route)

--------------------------------------------------------------------------------

Hold Paths: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout1 = PERIOD TIMEGRP
        "SciEngines_API_Core_api_clk_mgmt_up_clkout1" TS_CPI_CLK PHASE
        -0.416666667 ns HIGH 50%;
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvf
  ifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6
  (SLICE_X85Y133.CX), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.076ns (requirement - (clock path skew + uncertainty - data path))
  Source:               SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gco
    nvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_6 (FF)
  Destination:          SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gco
    nvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.459ns (Levels of Logic = 0)
  Clock Path Skew:      0.166ns (0.716 - 0.550)
  Source Clock:         SciEngines_API_Core/clk_int rising at 9.584ns
  Destination Clock:    api_clk rising at 9.584ns
  Clock Uncertainty:    0.217ns

```

```
564   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
565     Total System Jitter (TSJ):  0.070ns
566     Discrete Jitter (DJ):       0.181ns
567     Phase Error (PE):           0.120ns
568
569   Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_output_fifo/U0/x
      ↪ st_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_6 to
      ↪ SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/
      ↪ gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6
570     Location             Delay type         Delay(ns)  Physical Resource
571                                                        Logical Resource(s)
572     -------------------------------------------------  -------------------
573     SLICE_X83Y133.DQ     Tcko               0.198   SciEngines_API_Core/core/api_output_fi
        ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
574                                                      SciEngines_API_Core/core/api_output_f
                                                           ↪ ifo/U0/xst_fifo_generator/gcon
                                                           ↪ vfifo.rf/grf.rf/gntv_or_sync_f
                                                           ↪ ifo.gcx.clkx/wr_pntr_gc_6
575     SLICE_X85Y133.CX     net (fanout=1)        0.202
        ↪ SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.r
        ↪ f/gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
576     SLICE_X85Y133.CLK    Tckdi       (-Th)    -0.059
        ↪ SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.r
        ↪ f/gntv_or_sync_fifo.gcx.clkx/wr_q<1><7>
577                                        SciEngines_API_Core/core/api_output_fifo/U0/xst_f
                                                           ↪ ifo_generator/gconvfifo.rf/grf
                                                           ↪ .rf/gntv_or_sync_fifo.gcx.clkx
                                                           ↪ /gsync_stage[1].rd_stg_inst/Q_6
578     -------------------------------------------------  ---------------------------
579     Total                                     0.459ns (0.257ns logic, 0.202ns route)
580                                                        (56.0% logic, 44.0% route)
581
582 --------------------------------------------------------------------------------
583
584 Paths for end point SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfi
    ↪ fo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].wr_stg_inst/Q_4
    ↪ (SLICE_X97Y124.AX), 1 path
585 --------------------------------------------------------------------------------
586 Slack (hold path):      0.125ns (requirement - (clock path skew + uncertainty - data path))
587   Source:               SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon
      ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/rd_pntr_gc_4 (FF)
588   Destination:          SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon
      ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].wr_stg_inst/Q_4 (FF)
589   Requirement:          0.000ns
590   Data Path Delay:      0.506ns (Levels of Logic = 0)
591   Clock Path Skew:      0.164ns (0.800 - 0.636)
592   Source Clock:         SciEngines_API_Core/clk_int rising at 9.584ns
```

```
593   Destination Clock:    api_clk rising at 9.584ns
594   Clock Uncertainty:    0.217ns
595
596   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
597     Total System Jitter (TSJ):  0.070ns
598     Discrete Jitter (DJ):       0.181ns
599     Phase Error (PE):           0.120ns
600
601   Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_input_fifo/U0/xs
      ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/rd_pntr_gc_4 to
      ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/g
      ↪ ntv_or_sync_fifo.gcx.clkx/gsync_stage[1].wr_stg_inst/Q_4
602     Location             Delay type         Delay(ns)  Physical Resource
603                                                        Logical Resource(s)
604     -------------------------------------------------  -------------------
605     SLICE_X97Y126.CMUX   Tshcko               0.244   SciEngines_API_Core/core/api_input_fi
        ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/rd_q<0><5>
606                                                       SciEngines_API_Core/core/api_input_fi
                                                             ↪ fo/U0/xst_fifo_generator/gconv
                                                             ↪ fifo.rf/grf.rf/gntv_or_sync_fi
                                                             ↪ fo.gcx.clkx/rd_pntr_gc_4
607     SLICE_X97Y124.AX     net (fanout=1)        0.203
        ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf
        ↪ /gntv_or_sync_fifo.gcx.clkx/rd_q<0><4>
608     SLICE_X97Y124.CLK    Tckdi      (-Th)    -0.059   SciEngines_API_Core/core/api_input_fi
        ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/rd_q<1><7>
609                                          SciEngines_API_Core/core/api_input_fifo/U0/xst_f
                                                             ↪ ifo_generator/gconvfifo.rf/grf
                                                             ↪ .rf/gntv_or_sync_fifo.gcx.clkx
                                                             ↪ /gsync_stage[1].wr_stg_inst/Q_4
610     -------------------------------------------------  ---------------------------
611     Total                                       0.506ns (0.303ns logic, 0.203ns route)
612                                                         (59.9% logic, 40.1% route)
613
614 --------------------------------------------------------------------------------
615
616 Paths for end point SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvf
    ↪ ifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3
    ↪ (SLICE_X82Y133.DX), 1 path
617 --------------------------------------------------------------------------------
618 Slack (hold path):      0.141ns (requirement - (clock path skew + uncertainty - data path))
619   Source:               SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gco
      ↪ nvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_3 (FF)
620   Destination:          SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gco
      ↪ nvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3 (FF)
621   Requirement:          0.000ns
622   Data Path Delay:      0.524ns (Levels of Logic = 0)
```

```
623   Clock Path Skew:      0.166ns (0.716 - 0.550)
624   Source Clock:         SciEngines_API_Core/clk_int rising at 9.584ns
625   Destination Clock:    api_clk rising at 9.584ns
626   Clock Uncertainty:    0.217ns
627
628   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
629     Total System Jitter (TSJ):  0.070ns
630     Discrete Jitter (DJ):       0.181ns
631     Phase Error (PE):           0.120ns
632
633   Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_output_fifo/U0/x
      ↪  st_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_3 to
      ↪  SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/
      ↪  gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3
634     Location             Delay type         Delay(ns)  Physical Resource
635                                                        Logical Resource(s)
636     -------------------------------------------------  -------------------
637     SLICE_X83Y133.BQ     Tcko               0.198   SciEngines_API_Core/core/api_output_fi
        ↪  fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
638                                                      SciEngines_API_Core/core/api_output_f
                                                           ↪  ifo/U0/xst_fifo_generator/gcon
                                                           ↪  vfifo.rf/grf.rf/gntv_or_sync_f
                                                           ↪  ifo.gcx.clkx/wr_pntr_gc_3
639     SLICE_X82Y133.DX     net (fanout=1)        0.278
        ↪  SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.r
        ↪  f/gntv_or_sync_fifo.gcx.clkx/wr_q<0><3>
640     SLICE_X82Y133.CLK    Tckdi       (-Th)    -0.048
        ↪  SciEngines_API_Core/core/api_output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.r
        ↪  f/gntv_or_sync_fifo.gcx.clkx/wr_q<1><3>
641                                        SciEngines_API_Core/core/api_output_fifo/U0/xst_f
                                                           ↪  ifo_generator/gconvfifo.rf/grf
                                                           ↪  .rf/gntv_or_sync_fifo.gcx.clkx
                                                           ↪  /gsync_stage[1].rd_stg_inst/Q_3
642     -------------------------------------------------  ---------------------------
643     Total                                     0.524ns (0.246ns logic, 0.278ns route)
644                                                        (46.9% logic, 53.1% route)
645
646 --------------------------------------------------------------------------------
647
648 Component Switching Limit Checks: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout1 = PERIOD
    ↪  TIMEGRP
649         "SciEngines_API_Core_api_clk_mgmt_up_clkout1" TS_CPI_CLK PHASE
650         -0.416666667 ns HIGH 50%;
651 --------------------------------------------------------------------------------
652 Slack: 6.876ns (period - min period limit)
653   Period: 10.000ns
654   Min period limit: 3.124ns (320.102MHz) (Trper_CLKA(Fmax))
```

```
655   Physical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[0].gen_brams[29].bank_mem/CLKA
656   Logical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[0].gen_brams[29].bank_mem/CLKA
657   Location pin: RAMB16_X4Y40.CLKA
658   Clock network: api_clk
659 --------------------------------------------------------------------------------
660 Slack: 6.876ns (period - min period limit)
661   Period: 10.000ns
662   Min period limit: 3.124ns (320.102MHz) (Trper_CLKB(Fmax))
663   Physical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[0].gen_brams[29].bank_mem/CLKB
664   Logical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[0].gen_brams[29].bank_mem/CLKB
665   Location pin: RAMB16_X4Y40.CLKB
666   Clock network: api_clk
667 --------------------------------------------------------------------------------
668 Slack: 6.876ns (period - min period limit)
669   Period: 10.000ns
670   Min period limit: 3.124ns (320.102MHz) (Trper_CLKA(Fmax))
671   Physical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[1].gen_brams[16].bank_mem/CLKA
672   Logical resource:
      ↪  user_core/multi_core_system/shared_mem/gen_banks[1].gen_brams[16].bank_mem/CLKA
673   Location pin: RAMB16_X3Y62.CLKA
674   Clock network: api_clk
675 --------------------------------------------------------------------------------
676
677 ================================================================================
678 Timing constraint: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout0 = PERIOD
679 TIMEGRP         "SciEngines_API_Core_api_clk_mgmt_up_clkout0" TS_CPI_CLK PHASE
680        -0.416666667 ns HIGH 50%;
681 For more information, see Period Analysis in the Timing Closure User Guide (UG612).
682
683  164868 paths analyzed, 21547 endpoints analyzed, 0 failing endpoints
684  0 timing errors detected. (0 setup errors, 0 hold errors, 0 component switching limit
     ↪  errors)
685  Minimum period is   9.214ns.
686 --------------------------------------------------------------------------------
687
688 Paths for end point SciEngines_API_Core/core/led_out_0 (OLOGIC_X0Y127.D1), 5 paths
689 --------------------------------------------------------------------------------
690 Slack (setup path):     0.786ns (requirement - (data path - clock path skew + uncertainty))
691   Source:               user_core/state_2 (FF)
692   Destination:          SciEngines_API_Core/core/led_out_0 (FF)
693   Requirement:          10.000ns
694   Data Path Delay:      9.138ns (Levels of Logic = 1)
```

```
695   Clock Path Skew:      0.141ns (2.020 - 1.879)
696   Source Clock:         api_clk rising at -0.416ns
697   Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
698   Clock Uncertainty:    0.217ns
699
700   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
701     Total System Jitter (TSJ):  0.070ns
702     Discrete Jitter (DJ):       0.181ns
703     Phase Error (PE):           0.120ns
704
705   Maximum Data Path at Slow Process Corner: user_core/state_2 to
      ↪  SciEngines_API_Core/core/led_out_0
706     Location             Delay type         Delay(ns)  Physical Resource
707                                                        Logical Resource(s)
708     -------------------------------------------------  -------------------
709     SLICE_X94Y111.AQ     Tcko                  0.447   user_core/state<2>
710                                                        user_core/state_2
711     SLICE_X49Y131.A2     net (fanout=71)       4.413   user_core/state<2>
712     SLICE_X49Y131.A      Tilo                  0.259
        ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
713                                                        SciEngines_API_Core/core/mux121
714     OLOGIC_X0Y127.D1     net (fanout=1)        3.216
        ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
715     OLOGIC_X0Y127.CLK0   Todck                 0.803   SciEngines_API_Core/core/led_out<0>
716                                                        SciEngines_API_Core/core/led_out_0
717     -------------------------------------------------  --------------------------
718     Total                                      9.138ns (1.509ns logic, 7.629ns route)
719                                                        (16.5% logic, 83.5% route)
720
721 --------------------------------------------------------------------------------
722 Slack (setup path):     0.841ns (requirement - (data path - clock path skew + uncertainty))
723   Source:               user_core/state_1 (FF)
724   Destination:          SciEngines_API_Core/core/led_out_0 (FF)
725   Requirement:          10.000ns
726   Data Path Delay:      9.134ns (Levels of Logic = 1)
727   Clock Path Skew:      0.192ns (2.020 - 1.828)
728   Source Clock:         api_clk rising at -0.416ns
729   Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
730   Clock Uncertainty:    0.217ns
731
732   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
733     Total System Jitter (TSJ):  0.070ns
734     Discrete Jitter (DJ):       0.181ns
735     Phase Error (PE):           0.120ns
736
737   Maximum Data Path at Slow Process Corner: user_core/state_1 to
      ↪  SciEngines_API_Core/core/led_out_0
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X95Y112.CQ     Tcko                  0.391   user_core/state<1>
                                                       user_core/state_1
    SLICE_X49Y131.A1     net (fanout=124)      4.465   user_core/state<1>
    SLICE_X49Y131.A      Tilo                  0.259
      ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
                                                       SciEngines_API_Core/core/mux121
    OLOGIC_X0Y127.D1     net (fanout=1)        3.216
      ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
    OLOGIC_X0Y127.CLK0   Todck                 0.803   SciEngines_API_Core/core/led_out<0>
                                                       SciEngines_API_Core/core/led_out_0
    -------------------------------------------------  ---------------------------
    Total                                      9.134ns (1.453ns logic, 7.681ns route)
                                                       (15.9% logic, 84.1% route)

--------------------------------------------------------------------------------
Slack (setup path):     1.625ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/user_rst (FF)
  Destination:          SciEngines_API_Core/core/led_out_0 (FF)
  Requirement:          10.000ns
  Data Path Delay:      8.770ns (Levels of Logic = 1)
  Clock Path Skew:      0.492ns (1.202 - 0.710)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/core/user_rst to
    ↪  SciEngines_API_Core/core/led_out_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X98Y116.CQ     Tcko                  0.408   api_rst
                                                       SciEngines_API_Core/core/user_rst
    SLICE_X49Y131.A4     net (fanout=32)       4.084   api_rst
    SLICE_X49Y131.A      Tilo                  0.259
      ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
                                                       SciEngines_API_Core/core/mux121
    OLOGIC_X0Y127.D1     net (fanout=1)        3.216
      ↪  SciEngines_API_Core/core/led_proc.led[1]_led_in[1]_mux_21_OUT<0>
    OLOGIC_X0Y127.CLK0   Todck                 0.803   SciEngines_API_Core/core/led_out<0>
```

```
                                                          SciEngines_API_Core/core/led_out_0
    ------------------------------------------------  --------------------------
    Total                                     8.770ns (1.470ns logic, 7.300ns route)
                                                      (16.8% logic, 83.2% route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/channel_dn_prev/status_o_0
    (SLICE_X111Y127.AX), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     1.012ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/channel_dn_prev/link_up (FF)
  Destination:          SciEngines_API_Core/core/channel_dn_prev/status_o_0 (FF)
  Requirement:          10.000ns
  Data Path Delay:      8.816ns (Levels of Logic = 1)
  Clock Path Skew:      -0.075ns (0.695 - 0.770)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
    SciEngines_API_Core/core/channel_dn_prev/link_up to
    SciEngines_API_Core/core/channel_dn_prev/status_o_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X107Y110.BQ    Tcko                  0.391
      SciEngines_API_Core/core/channel_dn_prev/link_up
                                           SciEngines_API_Core/core/channel_dn_prev/link_up
    SLICE_X99Y73.A5      net (fanout=4)        3.687
      SciEngines_API_Core/core/channel_dn_prev/link_up
    SLICE_X99Y73.A       Tilo                  0.259
      SciEngines_API_Core/core/channel_dn_prev/link_up_rst_i_AND_538_o
                                                    SciEngines_API_Core/core/channel_dn_p
                                                       rev/link_up_rst_i_AND_538_o1
    SLICE_X111Y127.AX    net (fanout=1)        4.416
      SciEngines_API_Core/core/channel_dn_prev/link_up_rst_i_AND_538_o
    SLICE_X111Y127.CLK   Tdick                 0.063
      SciEngines_API_Core/core/channel_dn_prev/status_o<28>
                                                    SciEngines_API_Core/core/channel_dn_p
                                                       rev/status_o_0
    -------------------------------------------------  -------------------------
```

```
    Total                                     8.816ns (0.713ns logic, 8.103ns route)
                                                      (8.1% logic, 91.9% route)

--------------------------------------------------------------------------------
Slack (setup path):     3.267ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/channel_dn_prev/rst_i (FF)
  Destination:          SciEngines_API_Core/core/channel_dn_prev/status_o_0 (FF)
  Requirement:          10.000ns
  Data Path Delay:      6.559ns (Levels of Logic = 1)
  Clock Path Skew:      -0.077ns (0.784 - 0.861)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/core/channel_dn_prev/rst_i
    ↪  to SciEngines_API_Core/core/channel_dn_prev/status_o_0
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X90Y81.AQ      Tcko                  0.447
      ↪  SciEngines_API_Core/core/channel_dn_prev/rst_i
                                            SciEngines_API_Core/core/channel_dn_prev/rst_i
    SLICE_X99Y73.A1      net (fanout=39)       1.374
      ↪  SciEngines_API_Core/core/channel_dn_prev/rst_i
    SLICE_X99Y73.A       Tilo                  0.259
      ↪  SciEngines_API_Core/core/channel_dn_prev/link_up_rst_i_AND_538_o
                                                 SciEngines_API_Core/core/channel_dn_p⌋
                                                    ↪  rev/link_up_rst_i_AND_538_o1
    SLICE_X111Y127.AX    net (fanout=1)        4.416
      ↪  SciEngines_API_Core/core/channel_dn_prev/link_up_rst_i_AND_538_o
    SLICE_X111Y127.CLK   Tdick                 0.063
      ↪  SciEngines_API_Core/core/channel_dn_prev/status_o<28>
                                                 SciEngines_API_Core/core/channel_dn_p⌋
                                                    ↪  rev/status_o_0
    -------------------------------------------------  ---------------------------
    Total                                     6.559ns (0.769ns logic, 5.790ns route)
                                                      (11.7% logic, 88.3% route)

--------------------------------------------------------------------------------
```

```
Paths for end point SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17 (SLICE_X115Y76.B3), 5 paths
--------------------------------------------------------------------------------
Slack (setup path):     1.373ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_0 (FF)
  Destination:          SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17 (FF)
  Requirement:          10.000ns
  Data Path Delay:      8.522ns (Levels of Logic = 3)
  Clock Path Skew:      -0.008ns (0.243 - 0.251)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_0 to
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X123Y71.AQ     Tcko                  0.391
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count<0>
                                                       SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_0
    SLICE_X123Y71.B1     net (fanout=7)        0.439
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count<0>
    SLICE_X123Y71.B      Tilo                  0.259
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count<0>
```

```
879                                                   SciEngines_API_Core/core/channel_dn_p
                                                         ↪ rev/lane_out/input_fifo/U0/xst
                                                         ↪ _fifo_generator/gconvfifo.rf/g
                                                         ↪ rf.rf/gntv_or_sync_fifo.gl0.rd
                                                         ↪ /rpntr/Madd_gc0.count[3]_GND_2
                                                         ↪ 3_o_add_0_OUT_xor<0>11_INV_0
880     SLICE_X124Y95.C1     net (fanout=33)       4.081
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rd_pntr_plus1<0>_inv
881     SLICE_X124Y95.C      Tilo                  0.204
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
882                                                   SciEngines_API_Core/core/channel_dn_p
                                                         ↪ rev/lane_out/input_fifo/U0/xst
                                                         ↪ _fifo_generator/gconvfifo.rf/g
                                                         ↪ rf.rf/gntv_or_sync_fifo.mem/gd
                                                         ↪ m.dm/Mram_RAM3_RAMC_D1
883     SLICE_X115Y76.B3     net (fanout=1)        2.826
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
884     SLICE_X115Y76.CLK    Tas                   0.322
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i<19>
885                                                   SciEngines_API_Core/core/channel_dn_p
                                                         ↪ rev/lane_out/input_fifo/U0/xst
                                                         ↪ _fifo_generator/gconvfifo.rf/g
                                                         ↪ rf.rf/gntv_or_sync_fifo.mem/gd
                                                         ↪ m.dm/dout_i_17_dpot
886                                         SciEngines_API_Core/core/channel_dn_prev/lane_out/
                                                         ↪ input_fifo/U0/xst_fifo_generat
                                                         ↪ or/gconvfifo.rf/grf.rf/gntv_or
                                                         ↪ _sync_fifo.mem/gdm.dm/dout_i_17
887     ----------------------------------------------  ---------------------------
888     Total                                    8.522ns (1.176ns logic, 7.346ns route)
889                                                      (13.8% logic, 86.2% route)
890
891 --------------------------------------------------------------------------------
892 Slack (setup path):     3.319ns (requirement - (data path - clock path skew + uncertainty))
893   Source:               SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xs
      ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1_3
      ↪ (FF)
894   Destination:          SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xs
      ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17 (FF)
895   Requirement:          10.000ns
896   Data Path Delay:      6.575ns (Levels of Logic = 2)
897   Clock Path Skew:      -0.009ns (0.243 - 0.252)
898   Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
```

```
899 Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
900 Clock Uncertainty:    0.097ns
901
902 Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
903   Total System Jitter (TSJ):  0.070ns
904   Discrete Jitter (DJ):       0.181ns
905   Phase Error (PE):           0.000ns
906
907 Maximum Data Path at Slow Process Corner:
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/⌋
    ↪ gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1_3 to
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/⌋
    ↪ gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17
908   Location             Delay type         Delay(ns)  Physical Resource
909                                                        Logical Resource(s)
910   -------------------------------------------------  -------------------
911   SLICE_X126Y71.CQ     Tcko                  0.408
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
    ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1<3>
912                                                    SciEngines_API_Core/core/channel_dn_p⌋
                                                       ↪ rev/lane_out/input_fifo/U0/xst⌋
                                                       ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                       ↪ rf.rf/gntv_or_sync_fifo.gl0.rd⌋
                                                       ↪ /rpntr/gc0.count_d1_3
913   SLICE_X124Y95.C4     net (fanout=37)       2.815
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
    ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1<3>
914   SLICE_X124Y95.C      Tilo                  0.204
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
    ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
915                                                    SciEngines_API_Core/core/channel_dn_p⌋
                                                       ↪ rev/lane_out/input_fifo/U0/xst⌋
                                                       ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                       ↪ rf.rf/gntv_or_sync_fifo.mem/gd⌋
                                                       ↪ m.dm/Mram_RAM3_RAMC_D1
916   SLICE_X115Y76.B3     net (fanout=1)        2.826
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
    ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
917   SLICE_X115Y76.CLK    Tas                   0.322
    ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
    ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i<19>
918                                                    SciEngines_API_Core/core/channel_dn_p⌋
                                                       ↪ rev/lane_out/input_fifo/U0/xst⌋
                                                       ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                       ↪ rf.rf/gntv_or_sync_fifo.mem/gd⌋
                                                       ↪ m.dm/dout_i_17_dpot
```

```
                                          SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17
    ----------------------------------------------------  -------------------------
    Total                                          6.575ns (0.934ns logic, 5.641ns route)
                                                           (14.2% logic, 85.8% route)

--------------------------------------------------------------------------------
Slack (setup path):     3.865ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1_1 (FF)
  Destination:          SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17 (FF)
  Requirement:          10.000ns
  Data Path Delay:      6.029ns (Levels of Logic = 2)
  Clock Path Skew:      -0.009ns (0.243 - 0.252)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1_1 to
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i_17
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X126Y71.AQ     Tcko                  0.408
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1<3>
                                                       SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1_1
    SLICE_X124Y95.C2     net (fanout=34)       2.269
  SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gl0.rd/rpntr/gc0.count_d1<1>
```

```
947     SLICE_X124Y95.C      Tilo                  0.204
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
948                                                   SciEngines_API_Core/core/channel_dn_p⌋
                                                         ↪ rev/lane_out/input_fifo/U0/xst⌋
                                                         ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                         ↪ rf.rf/gntv_or_sync_fifo.mem/gd⌋
                                                         ↪ m.dm/Mram_RAM3_RAMC_D1
949     SLICE_X115Y76.B3     net (fanout=1)        2.826
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<17>
950     SLICE_X115Y76.CLK    Tas                   0.322
        ↪ SciEngines_API_Core/core/channel_dn_prev/lane_out/input_fifo/U0/xst_fifo_generato⌋
        ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/dout_i<19>
951                                                   SciEngines_API_Core/core/channel_dn_p⌋
                                                         ↪ rev/lane_out/input_fifo/U0/xst⌋
                                                         ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                         ↪ rf.rf/gntv_or_sync_fifo.mem/gd⌋
                                                         ↪ m.dm/dout_i_17_dpot
952                                        SciEngines_API_Core/core/channel_dn_prev/lane_out/⌋
                                                         ↪ input_fifo/U0/xst_fifo_generat⌋
                                                         ↪ or/gconvfifo.rf/grf.rf/gntv_or⌋
                                                         ↪ _sync_fifo.mem/gdm.dm/dout_i_17
953     ------------------------------------------------  ---------------------------
954     Total                                     6.029ns (0.934ns logic, 5.095ns route)
955                                                       (15.5% logic, 84.5% route)
956
957 --------------------------------------------------------------------------------
958
959 Hold Paths: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout0 = PERIOD TIMEGRP
960         "SciEngines_API_Core_api_clk_mgmt_up_clkout0" TS_CPI_CLK PHASE
961         -0.416666667 ns HIGH 50%;
962 --------------------------------------------------------------------------------
963
964 Paths for end point SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfi⌋
    ↪ fo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_7
    ↪ (SLICE_X82Y128.DX), 1 path
965 --------------------------------------------------------------------------------
966 Slack (hold path):      0.045ns (requirement - (clock path skew + uncertainty - data path))
967   Source:               SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon⌋
      ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_7 (FF)
968   Destination:          SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon⌋
      ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_7 (FF)
969   Requirement:          0.000ns
970   Data Path Delay:      0.428ns (Levels of Logic = 0)
971   Clock Path Skew:      0.166ns (0.724 - 0.558)
972   Source Clock:         api_clk rising at 9.584ns
```

```
  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
  Clock Uncertainty:    0.217ns

  Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.120ns

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_7 to SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X83Y129.AQ     Tcko                  0.198   SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><7>
                                                       SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_7
    SLICE_X82Y128.DX     net (fanout=1)        0.182
                                                       SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><7>
    SLICE_X82Y128.CLK    Tckdi      (-Th)    -0.048   SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<1><7>
                                                       SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_7
    -------------------------------------------------  ---------------------------
    Total                                      0.428ns (0.246ns logic, 0.182ns route)
                                                       (57.5% logic, 42.5% route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6
  (SLICE_X82Y128.CX), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.095ns (requirement - (clock path skew + uncertainty - data path))
  Source:               SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_6 (FF)
  Destination:          SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6 (FF)
  Requirement:          0.000ns
  Data Path Delay:      0.477ns (Levels of Logic = 0)
```

```
1003  Clock Path Skew:      0.165ns (0.724 - 0.559)
1004  Source Clock:         api_clk rising at 9.584ns
1005  Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
1006  Clock Uncertainty:    0.217ns
1007
1008  Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1009    Total System Jitter (TSJ):  0.070ns
1010    Discrete Jitter (DJ):       0.181ns
1011    Phase Error (PE):           0.120ns
1012
1013  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_input_fifo/U0/xs
      ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_6 to
      ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/g
      ↪ ntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_6
1014    Location             Delay type         Delay(ns)  Physical Resource
1015                                                       Logical Resource(s)
1016    -------------------------------------------------  -------------------
1017    SLICE_X84Y128.DQ     Tcko                  0.234   SciEngines_API_Core/core/api_input_fi
        ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
1018                                                     SciEngines_API_Core/core/api_input_fi
                                                           ↪ fo/U0/xst_fifo_generator/gconv
                                                           ↪ fifo.rf/grf.rf/gntv_or_sync_fi
                                                           ↪ fo.gcx.clkx/wr_pntr_gc_6
1019    SLICE_X82Y128.CX     net (fanout=1)        0.195
        ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf
        ↪ /gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
1020    SLICE_X82Y128.CLK    Tckdi      (-Th)    -0.048   SciEngines_API_Core/core/api_input_fi
        ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<1><7>
1021                                           SciEngines_API_Core/core/api_input_fifo/U0/xst_f
                                                           ↪ ifo_generator/gconvfifo.rf/grf
                                                           ↪ .rf/gntv_or_sync_fifo.gcx.clkx
                                                           ↪ /gsync_stage[1].rd_stg_inst/Q_6
1022    -------------------------------------------------  ---------------------------
1023    Total                                       0.477ns (0.282ns logic, 0.195ns route)
1024                                                       (59.1% logic, 40.9% route)
1025
1026 --------------------------------------------------------------------------------
1027
1028 Paths for end point SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfi
     ↪ fo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3
     ↪ (SLICE_X85Y128.DX), 1 path
1029 --------------------------------------------------------------------------------
1030 Slack (hold path):      0.101ns (requirement - (clock path skew + uncertainty - data path))
1031   Source:               SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon
       ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_3 (FF)
1032   Destination:          SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gcon
       ↪ vfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3 (FF)
```

```
1033   Requirement:          0.000ns
1034   Data Path Delay:      0.483ns (Levels of Logic = 0)
1035   Clock Path Skew:      0.165ns (0.724 - 0.559)
1036   Source Clock:         api_clk rising at 9.584ns
1037   Destination Clock:    SciEngines_API_Core/clk_int rising at 9.584ns
1038   Clock Uncertainty:    0.217ns
1039
1040   Clock Uncertainty:          0.217ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1041     Total System Jitter (TSJ):  0.070ns
1042     Discrete Jitter (DJ):       0.181ns
1043     Phase Error (PE):           0.120ns
1044
1045   Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/api_input_fifo/U0/xs
       ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_pntr_gc_3 to
       ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/g
       ↪ ntv_or_sync_fifo.gcx.clkx/gsync_stage[1].rd_stg_inst/Q_3
1046     Location             Delay type         Delay(ns)  Physical Resource
1047                                                        Logical Resource(s)
1048     -------------------------------------------------  -------------------
1049     SLICE_X84Y128.BQ     Tcko                  0.234   SciEngines_API_Core/core/api_input_fi
         ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<0><6>
1050                                                       SciEngines_API_Core/core/api_input_fi
                                                             ↪ fo/U0/xst_fifo_generator/gconv
                                                             ↪ fifo.rf/grf.rf/gntv_or_sync_fi
                                                             ↪ fo.gcx.clkx/wr_pntr_gc_3
1051     SLICE_X85Y128.DX     net (fanout=1)        0.190
         ↪ SciEngines_API_Core/core/api_input_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf
         ↪ /gntv_or_sync_fifo.gcx.clkx/wr_q<0><3>
1052     SLICE_X85Y128.CLK    Tckdi      (-Th)    -0.059   SciEngines_API_Core/core/api_input_fi
         ↪ fo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.gcx.clkx/wr_q<1><3>
1053                                          SciEngines_API_Core/core/api_input_fifo/U0/xst_f
                                                             ↪ ifo_generator/gconvfifo.rf/grf
                                                             ↪ .rf/gntv_or_sync_fifo.gcx.clkx
                                                             ↪ /gsync_stage[1].rd_stg_inst/Q_3
1054     -------------------------------------------------  ---------------------------
1055     Total                                      0.483ns (0.293ns logic, 0.190ns route)
1056                                                        (60.7% logic, 39.3% route)
1057
1058 --------------------------------------------------------------------------------
1059
1060 Component Switching Limit Checks: TS_SciEngines_API_Core_api_clk_mgmt_up_clkout0 = PERIOD
     ↪ TIMEGRP
1061         "SciEngines_API_Core_api_clk_mgmt_up_clkout0" TS_CPI_CLK PHASE
1062         -0.416666667 ns HIGH 50%;
1063 --------------------------------------------------------------------------------
1064 Slack: 6.876ns (period - min period limit)
1065   Period: 10.000ns
```

```
1066   Min period limit: 3.124ns (320.102MHz) (Trper_CLKA(Fmax))
1067   Physical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.
       ↪  Input_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg
       ↪  .gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[3].ram.r/s6_noini
       ↪  t.ram/SDP.WIDE_PRIM9.ram/CLKAWRCLK
1068   Logical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.I
       ↪  nput_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg.
       ↪  gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[3].ram.r/s6_noinit
       ↪  .ram/SDP.WIDE_PRIM9.ram/CLKAWRCLK
1069   Location pin: RAMB8_X4Y75.CLKAWRCLK
1070   Clock network: SciEngines_API_Core/clk_int
1071 --------------------------------------------------------------------------------
1072 Slack: 6.876ns (period - min period limit)
1073   Period: 10.000ns
1074   Min period limit: 3.124ns (320.102MHz) (Trper_CLKB(Fmax))
1075   Physical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.
       ↪  Input_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg
       ↪  .gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[3].ram.r/s6_noini
       ↪  t.ram/SDP.WIDE_PRIM9.ram/CLKBRDCLK
1076   Logical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.I
       ↪  nput_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg.
       ↪  gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[3].ram.r/s6_noinit
       ↪  .ram/SDP.WIDE_PRIM9.ram/CLKBRDCLK
1077   Location pin: RAMB8_X4Y75.CLKBRDCLK
1078   Clock network: SciEngines_API_Core/clk_int
1079 --------------------------------------------------------------------------------
1080 Slack: 6.876ns (period - min period limit)
1081   Period: 10.000ns
1082   Min period limit: 3.124ns (320.102MHz) (Trper_CLKA(Fmax))
1083   Physical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.
       ↪  Input_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg
       ↪  .gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[2].ram.r/s6_noini
       ↪  t.ram/SDP.WIDE_PRIM9.ram/CLKAWRCLK
1084   Logical resource: SciEngines_API_Core/core/channel_up_next/user_input/input_fifo_bram.I
       ↪  nput_FIFO/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gbm.gbmg.
       ↪  gbmga.ngecc.bmg/gnativebmg.native_blk_mem_gen/valid.cstr/ramloop[2].ram.r/s6_noinit
       ↪  .ram/SDP.WIDE_PRIM9.ram/CLKAWRCLK
1085   Location pin: RAMB8_X4Y71.CLKAWRCLK
1086   Clock network: SciEngines_API_Core/clk_int
1087 --------------------------------------------------------------------------------
1088
1089 ================================================================================
1090 Timing constraint: TS_SciEngines_API_Core_api_clk_mgmt_dn_clkout1 = PERIOD
1091 TIMEGRP         "SciEngines_API_Core_api_clk_mgmt_dn_clkout1" TS_CNI_CLK PHASE
1092        -0.416666667 ns HIGH 50%;
1093 For more information, see Period Analysis in the Timing Closure User Guide (UG612).
1094
```

```
 3001 paths analyzed, 2163 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors, 0 component switching limit errors)
 Minimum period is   7.954ns.
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1 (SLICE_X98Y185.B1), 10 paths
--------------------------------------------------------------------------------
Slack (setup path):     2.046ns (requirement - (data path - clock path skew + uncertainty))
  Source:               SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 (FF)
  Destination:          SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1 (FF)
  Requirement:          10.000ns
  Data Path Delay:      7.843ns (Levels of Logic = 4)
  Clock Path Skew:      -0.014ns (0.145 - 0.159)
  Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 to SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X99Y187.DQ     Tcko                  0.391   SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11
    SLICE_X77Y181.C3     net (fanout=3)        2.619   SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
    SLICE_X77Y181.CMUX   Tilo                  0.313   SciEngines_API_Core/N128
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1_SW0
    SLICE_X77Y181.A2     net (fanout=1)        0.605   SciEngines_API_Core/N138
    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
```

```
1128                                                SciEngines_API_Core/core/channel_up_next/la⌋
                                                      ↪ ne_in/com_lanes_in[0].lane/lan⌋
                                                      ↪ e_i[16]_GND_19_o_equal_6_o<16>1
1129    SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up⌋
      ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
1130    SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_⌋
      ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1131                                              SciEngines_API_Core/core/channel_up_next/lan⌋
                                                      ↪ e_in/com_lanes_in[0].lane/lane⌋
                                                      ↪ _i[16]_GND_19_o_equal_6_o<16>21
1132    SLICE_X98Y185.B1     net (fanout=2)        0.458   SciEngines_API_Core/core/channel_up⌋
      ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
1133    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_⌋
      ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1134                                         SciEngines_API_Core/core/channel_up_next/lane_in⌋
                                                      ↪ /com_lanes_in[0].lane/Mmux_GND⌋
                                                      ↪ _19_o_chunk_passed[0]_MUX_69_o1
1135                                                SciEngines_API_Core/core/channel_up_n⌋
                                                      ↪ ext/lane_in/com_lanes_in[0].la⌋
                                                      ↪ ne/chunk_passed_1
1136    ------------------------------------------------  ---------------------------
1137    Total                                      7.843ns (1.509ns logic, 6.334ns route)
1138                                                       (19.2% logic, 80.8% route)
1139
1140 --------------------------------------------------------------------------------
1141 Slack (setup path):     2.859ns (requirement - (data path - clock path skew + uncertainty))
1142   Source:
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 (FF)
1143   Destination:
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1
      ↪ (FF)
1144   Requirement:          10.000ns
1145   Data Path Delay:      7.026ns (Levels of Logic = 3)
1146   Clock Path Skew:      -0.018ns (0.233 - 0.251)
1147   Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
1148   Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
1149   Clock Uncertainty:    0.097ns
1150
1151   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1152     Total System Jitter (TSJ):  0.070ns
1153     Discrete Jitter (DJ):       0.181ns
1154     Phase Error (PE):           0.000ns
1155
1156   Maximum Data Path at Slow Process Corner:
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 to
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1
1157     Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                    Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X100Y187.DQ    Tcko                  0.447
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
                                          SciEngines_API_Core/core/channel_up_next/lane_in
                                                    ↪ /com_lanes_in[0].lane/lane_i_15
    SLICE_X77Y181.A3     net (fanout=3)        2.664
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
                                                SciEngines_API_Core/core/channel_up_next/la
                                                    ↪ ne_in/com_lanes_in[0].lane/lan
                                                    ↪ e_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                              SciEngines_API_Core/core/channel_up_next/lan
                                                    ↪ e_in/com_lanes_in[0].lane/lane
                                                    ↪ _i[16]_GND_19_o_equal_6_o<16>21
    SLICE_X98Y185.B1     net (fanout=2)        0.458   SciEngines_API_Core/core/channel_up
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                          SciEngines_API_Core/core/channel_up_next/lane_in
                                                    ↪ /com_lanes_in[0].lane/Mmux_GND
                                                    ↪ _19_o_chunk_passed[0]_MUX_69_o1
                                                SciEngines_API_Core/core/channel_up_n
                                                    ↪ ext/lane_in/com_lanes_in[0].la
                                                    ↪ ne/chunk_passed_1
    -------------------------------------------------  ---------------------------
    Total                                      7.026ns (1.252ns logic, 5.774ns route)
                                                    (17.8% logic, 82.2% route)

--------------------------------------------------------------------------------
Slack (setup path):     3.053ns (requirement - (data path - clock path skew + uncertainty))
  Source:
  ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 (FF)
  Destination:
  ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1
  ↪ (FF)
  Requirement:          10.000ns
  Data Path Delay:      6.832ns (Levels of Logic = 3)
  Clock Path Skew:      -0.018ns (0.145 - 0.163)
  Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.097ns
```

```
1187  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1188    Total System Jitter (TSJ):  0.070ns
1189    Discrete Jitter (DJ):       0.181ns
1190    Phase Error (PE):           0.000ns
1191
1192  Maximum Data Path at Slow Process Corner:
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 to
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_1
1193    Location             Delay type         Delay(ns)  Physical Resource
1194                                                       Logical Resource(s)
1195    -------------------------------------------------  -------------------
1196    SLICE_X99Y190.DQ     Tcko                  0.391
        ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
1197                                          SciEngines_API_Core/core/channel_up_next/lane_i⌋
                                                         ↪ n/com_lanes_in[0].lane/lane_i_3
1198    SLICE_X77Y181.A5     net (fanout=3)        2.526
        ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
1199    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
1200                                         SciEngines_API_Core/core/channel_up_next/la⌋
                                                         ↪ ne_in/com_lanes_in[0].lane/lan⌋
                                                         ↪ e_i[16]_GND_19_o_equal_6_o<16>1
1201    SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up⌋
        ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
1202    SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_⌋
        ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1203                                          SciEngines_API_Core/core/channel_up_next/lan⌋
                                                         ↪ e_in/com_lanes_in[0].lane/lane⌋
                                                         ↪ _i[16]_GND_19_o_equal_6_o<16>21
1204    SLICE_X98Y185.B1     net (fanout=2)        0.458   SciEngines_API_Core/core/channel_up⌋
        ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
1205    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_⌋
        ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1206                                       SciEngines_API_Core/core/channel_up_next/lane_in⌋
                                                         ↪ /com_lanes_in[0].lane/Mmux_GND⌋
                                                         ↪ _19_o_chunk_passed[0]_MUX_69_o1
1207                                                  SciEngines_API_Core/core/channel_up_n⌋
                                                         ↪ ext/lane_in/com_lanes_in[0].la⌋
                                                         ↪ ne/chunk_passed_1
1208    -------------------------------------------------  ---------------------------
1209    Total                                      6.832ns (1.196ns logic, 5.636ns route)
1210                                                       (17.5% logic, 82.5% route)
1211
1212 --------------------------------------------------------------------------------
1213
1214 Paths for end point
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
      ↪ (SLICE_X98Y185.C6), 10 paths
```

```
1215 ------------------------------------------------------------------------------------
1216 Slack (setup path):     2.380ns (requirement - (data path - clock path skew + uncertainty))
1217   Source:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 (FF)
1218   Destination:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
       ↪ (FF)
1219   Requirement:          10.000ns
1220   Data Path Delay:      7.509ns (Levels of Logic = 4)
1221   Clock Path Skew:      -0.014ns (0.145 - 0.159)
1222   Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
1223   Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
1224   Clock Uncertainty:    0.097ns
1225
1226   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1227     Total System Jitter (TSJ):  0.070ns
1228     Discrete Jitter (DJ):       0.181ns
1229     Phase Error (PE):           0.000ns
1230
1231   Maximum Data Path at Slow Process Corner:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 to
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1232     Location             Delay type         Delay(ns)  Physical Resource
1233                                                        Logical Resource(s)
1234     -------------------------------------------------  -------------------
1235     SLICE_X99Y187.DQ     Tcko                  0.391
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
1236                                       SciEngines_API_Core/core/channel_up_next/lane_in⌋
                                             ↪ /com_lanes_in[0].lane/lane_i_11
1237     SLICE_X77Y181.C3     net (fanout=3)        2.619
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
1238     SLICE_X77Y181.CMUX   Tilo                  0.313   SciEngines_API_Core/N128
1239                                      SciEngines_API_Core/core/channel_up_next/lane_i⌋
                                             ↪ n/com_lanes_in[0].lane/lane_i[⌋
                                             ↪ 16]_GND_19_o_equal_6_o<16>1_SW0
1240     SLICE_X77Y181.A2     net (fanout=1)        0.605   SciEngines_API_Core/N138
1241     SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
1242                                         SciEngines_API_Core/core/channel_up_next/la⌋
                                             ↪ ne_in/com_lanes_in[0].lane/lan⌋
                                             ↪ e_i[16]_GND_19_o_equal_6_o<16>1
1243     SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up⌋
         ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
1244     SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_⌋
         ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
1245                                         SciEngines_API_Core/core/channel_up_next/lan⌋
                                             ↪ e_in/com_lanes_in[0].lane/lane⌋
                                             ↪ _i[16]_GND_19_o_equal_6_o<16>21
```

```
    SLICE_X98Y185.C6     net (fanout=2)        0.124   SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/Mmux_GND_19_o_chunk_passed[1]_MUX_70_o1
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
    ----------------------------------------------------  ---------------------------
    Total                                          7.509ns (1.509ns logic, 6.000ns route)
                                                           (20.1% logic, 79.9% route)

--------------------------------------------------------------------------------
Slack (setup path):     3.193ns (requirement - (data path - clock path skew + uncertainty))
  Source:
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 (FF)
  Destination:
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
    (FF)
  Requirement:          10.000ns
  Data Path Delay:      6.692ns (Levels of Logic = 3)
  Clock Path Skew:      -0.018ns (0.233 - 0.251)
  Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 to
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ----------------------------------------------------  -------------------
    SLICE_X100Y187.DQ    Tcko                  0.447
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15
    SLICE_X77Y181.A3     net (fanout=3)        2.664
    SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
```

```
                                                    SciEngines_API_Core/core/channel_up_next/la
                                                      ↪ ne_in/com_lanes_in[0].lane/lan
                                                      ↪ e_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                                  SciEngines_API_Core/core/channel_up_next/lan
                                                      ↪ e_in/com_lanes_in[0].lane/lane
                                                      ↪ _i[16]_GND_19_o_equal_6_o<16>21
    SLICE_X98Y185.C6     net (fanout=2)        0.124   SciEngines_API_Core/core/channel_up
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                             SciEngines_API_Core/core/channel_up_next/lane_in
                                                      ↪ /com_lanes_in[0].lane/Mmux_GND
                                                      ↪ _19_o_chunk_passed[1]_MUX_70_o1
                                                   SciEngines_API_Core/core/channel_up_n
                                                      ↪ ext/lane_in/com_lanes_in[0].la
                                                      ↪ ne/chunk_passed_2
    ------------------------------------------------  ---------------------------
    Total                                      6.692ns (1.252ns logic, 5.440ns route)
                                                       (18.7% logic, 81.3% route)

--------------------------------------------------------------------------------
Slack (setup path):     3.387ns (requirement - (data path - clock path skew + uncertainty))
  Source:
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 (FF)
  Destination:
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
    ↪ (FF)
  Requirement:          10.000ns
  Data Path Delay:      6.498ns (Levels of Logic = 3)
  Clock Path Skew:      -0.018ns (0.145 - 0.163)
  Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.097ns

  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.000ns

  Maximum Data Path at Slow Process Corner:
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 to
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_2
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                    Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X99Y190.DQ     Tcko                  0.391
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
                                          SciEngines_API_Core/core/channel_up_next/lane_i┘
                                                    ↪ n/com_lanes_in[0].lane/lane_i_3
    SLICE_X77Y181.A5     net (fanout=3)        2.526
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
                                         SciEngines_API_Core/core/channel_up_next/la┘
                                                    ↪ ne_in/com_lanes_in[0].lane/lan┘
                                                    ↪ e_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D2     net (fanout=2)        2.652   SciEngines_API_Core/core/channel_up┘
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
    SLICE_X98Y185.D      Tilo                  0.205   SciEngines_API_Core/core/channel_up_┘
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                         SciEngines_API_Core/core/channel_up_next/lan┘
                                                    ↪ e_in/com_lanes_in[0].lane/lane┘
                                                    ↪ _i[16]_GND_19_o_equal_6_o<16>21
    SLICE_X98Y185.C6     net (fanout=2)        0.124   SciEngines_API_Core/core/channel_up┘
    ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>2
    SLICE_X98Y185.CLK    Tas                   0.341   SciEngines_API_Core/core/channel_up_┘
    ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_2
                                          SciEngines_API_Core/core/channel_up_next/lane_in┘
                                                    ↪ /com_lanes_in[0].lane/Mmux_GND┘
                                                    ↪ _19_o_chunk_passed[1]_MUX_70_o1
                                                SciEngines_API_Core/core/channel_up_n┘
                                                    ↪ ext/lane_in/com_lanes_in[0].la┘
                                                    ↪ ne/chunk_passed_2
    -------------------------------------------------  ---------------------------
    Total                                      6.498ns (1.196ns logic, 5.302ns route)
                                                    (18.4% logic, 81.6% route)

--------------------------------------------------------------------------------

Paths for end point
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
    ↪ (SLICE_X99Y185.B4), 7 paths
--------------------------------------------------------------------------------
Slack (setup path):     2.846ns (requirement - (data path - clock path skew + uncertainty))
  Source:
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 (FF)
  Destination:
    ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
    ↪ (FF)
  Requirement:          10.000ns
  Data Path Delay:      7.043ns (Levels of Logic = 3)
```

```
1335  Clock Path Skew:      -0.014ns (0.145 - 0.159)
1336  Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
1337  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
1338  Clock Uncertainty:    0.097ns
1339
1340  Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1341    Total System Jitter (TSJ):  0.070ns
1342    Discrete Jitter (DJ):       0.181ns
1343    Phase Error (PE):           0.000ns
1344
1345  Maximum Data Path at Slow Process Corner:
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_11 to
      ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
1346    Location             Delay type         Delay(ns)  Physical Resource
1347                                                       Logical Resource(s)
1348    -------------------------------------------------  -------------------
1349    SLICE_X99Y187.DQ     Tcko                  0.391
        ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
1350                                       SciEngines_API_Core/core/channel_up_next/lane_in
                                                       ↪ /com_lanes_in[0].lane/lane_i_11
1351    SLICE_X77Y181.C3     net (fanout=3)        2.619
        ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<11>
1352    SLICE_X77Y181.CMUX   Tilo                  0.313   SciEngines_API_Core/N128
1353                                      SciEngines_API_Core/core/channel_up_next/lane_i
                                                       ↪ n/com_lanes_in[0].lane/lane_i[
                                                       ↪ 16]_GND_19_o_equal_6_o<16>1_SW0
1354    SLICE_X77Y181.A2     net (fanout=1)        0.605   SciEngines_API_Core/N138
1355    SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
1356                                         SciEngines_API_Core/core/channel_up_next/la
                                                       ↪ ne_in/com_lanes_in[0].lane/lan
                                                       ↪ e_i[16]_GND_19_o_equal_6_o<16>1
1357    SLICE_X99Y185.B4     net (fanout=2)        2.534   SciEngines_API_Core/core/channel_up
        ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
1358    SLICE_X99Y185.CLK    Tas                   0.322   SciEngines_API_Core/core/channel_up_
        ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_3
1359                                       SciEngines_API_Core/core/channel_up_next/lane_in/
                                                       ↪ com_lanes_in[0].lane/Mmux_GND_
                                                       ↪ 19_o_chunk_passed[2]_MUX_71_o11
1360                                            SciEngines_API_Core/core/channel_up_n
                                                       ↪ ext/lane_in/com_lanes_in[0].la
                                                       ↪ ne/chunk_passed_3
1361    -------------------------------------------------  ---------------------------
1362    Total                                      7.043ns (1.285ns logic, 5.758ns route)
1363                                                       (18.2% logic, 81.8% route)
1364
1365 --------------------------------------------------------------------------------
1366 Slack (setup path):     3.659ns (requirement - (data path - clock path skew + uncertainty))
```

```
Source:
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 (FF)
Destination:
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
  (FF)
Requirement:          10.000ns
Data Path Delay:      6.226ns (Levels of Logic = 2)
Clock Path Skew:      -0.018ns (0.233 - 0.251)
Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
Clock Uncertainty:    0.097ns

Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.070ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.000ns

Maximum Data Path at Slow Process Corner:
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_15 to
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  SLICE_X100Y187.DQ    Tcko                  0.447
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
                                       SciEngines_API_Core/core/channel_up_next/lane_in
                                                     /com_lanes_in[0].lane/lane_i_15
  SLICE_X77Y181.A3     net (fanout=3)        2.664
  SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<15>
  SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
                                            SciEngines_API_Core/core/channel_up_next/la
                                                     ne_in/com_lanes_in[0].lane/lan
                                                     e_i[16]_GND_19_o_equal_6_o<16>1
  SLICE_X99Y185.B4     net (fanout=2)        2.534   SciEngines_API_Core/core/channel_up
  _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
  SLICE_X99Y185.CLK    Tas                   0.322   SciEngines_API_Core/core/channel_up_
  next/lane_in/com_lanes_in[0].lane/chunk_passed_3
                                       SciEngines_API_Core/core/channel_up_next/lane_in/
                                                     com_lanes_in[0].lane/Mmux_GND_
                                                     19_o_chunk_passed[2]_MUX_71_o11
                                                  SciEngines_API_Core/core/channel_up_n
                                                     ext/lane_in/com_lanes_in[0].la
                                                     ne/chunk_passed_3
  -------------------------------------------------  ---------------------------
  Total                                      6.226ns (1.028ns logic, 5.198ns route)
                                                     (16.5% logic, 83.5% route)

```

```
1398 ------------------------------------------------------------------------------------
1399 Slack (setup path):     3.853ns (requirement - (data path - clock path skew + uncertainty))
1400   Source:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 (FF)
1401   Destination:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
       ↪ (FF)
1402   Requirement:          10.000ns
1403   Data Path Delay:      6.032ns (Levels of Logic = 2)
1404   Clock Path Skew:      -0.018ns (0.145 - 0.163)
1405   Source Clock:         SciEngines_API_Core/cni_dom rising at -0.416ns
1406   Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
1407   Clock Uncertainty:    0.097ns
1408
1409   Clock Uncertainty:          0.097ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1410     Total System Jitter (TSJ):  0.070ns
1411     Discrete Jitter (DJ):       0.181ns
1412     Phase Error (PE):           0.000ns
1413
1414   Maximum Data Path at Slow Process Corner:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i_3 to
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/chunk_passed_3
1415     Location             Delay type         Delay(ns)  Physical Resource
1416                                                        Logical Resource(s)
1417     -------------------------------------------------  -------------------
1418     SLICE_X99Y190.DQ     Tcko                  0.391
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
1419                                          SciEngines_API_Core/core/channel_up_next/lane_i⌋
                                                  ↪ n/com_lanes_in[0].lane/lane_i_3
1420     SLICE_X77Y181.A5     net (fanout=3)        2.526
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/com_lanes_in[0].lane/lane_i<3>
1421     SLICE_X77Y181.A      Tilo                  0.259   SciEngines_API_Core/N128
1422                                                SciEngines_API_Core/core/channel_up_next/la⌋
                                                  ↪ ne_in/com_lanes_in[0].lane/lan⌋
                                                  ↪ e_i[16]_GND_19_o_equal_6_o<16>1
1423     SLICE_X99Y185.B4     net (fanout=2)        2.534   SciEngines_API_Core/core/channel_up⌋
         ↪ _next/lane_in/com_lanes_in[0].lane/lane_i[16]_GND_19_o_equal_6_o<16>1
1424     SLICE_X99Y185.CLK    Tas                   0.322   SciEngines_API_Core/core/channel_up_⌋
         ↪ next/lane_in/com_lanes_in[0].lane/chunk_passed_3
1425                                          SciEngines_API_Core/core/channel_up_next/lane_in/⌋
                                                  ↪ com_lanes_in[0].lane/Mmux_GND_⌋
                                                  ↪ 19_o_chunk_passed[2]_MUX_71_o11
1426                                                SciEngines_API_Core/core/channel_up_n⌋
                                                  ↪ ext/lane_in/com_lanes_in[0].la⌋
                                                  ↪ ne/chunk_passed_3
1427     -------------------------------------------------  ---------------------------
1428     Total                                     6.032ns (0.972ns logic, 5.060ns route)
```

```
                                                        (16.1% logic, 83.9% route)

--------------------------------------------------------------------------------

Hold Paths: TS_SciEngines_API_Core_api_clk_mgmt_dn_clkout1 = PERIOD TIMEGRP
        "SciEngines_API_Core_api_clk_mgmt_dn_clkout1" TS_CNI_CLK PHASE
        -0.416666667 ns HIGH 50%;
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMB_D1 (SLICE_X104Y178.BI), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.307ns (requirement - (clock path skew + uncertainty - data path))
  Source:               SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_21 (FF)
  Destination:          SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMB_D1 (RAM)
  Requirement:          0.000ns
  Data Path Delay:      0.311ns (Levels of Logic = 0)
  Clock Path Skew:      0.004ns (0.043 - 0.039)
  Source Clock:         SciEngines_API_Core/cni_dom rising at 9.584ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_21 to SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMB_D1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X105Y179.BQ    Tcko                  0.198
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<23>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_21
    SLICE_X104Y178.BI    net (fanout=1)        0.113
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<21>
    SLICE_X104Y178.CLK   Tdh         (-Th)     0.000
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<23>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMB_D1
    -------------------------------------------------  -------------------------
```

```
    Total                                          0.311ns (0.198ns logic, 0.113ns route)
                                                           (63.7% logic, 36.3% route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMC (SLICE_X104Y178.CX), 1 path
--------------------------------------------------------------------------------
Slack (hold path):      0.310ns (requirement - (clock path skew + uncertainty - data path))
  Source:               SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_22 (FF)
  Destination:          SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMC (RAM)
  Requirement:          0.000ns
  Data Path Delay:      0.314ns (Levels of Logic = 0)
  Clock Path Skew:      0.004ns (0.043 - 0.039)
  Source Clock:         SciEngines_API_Core/cni_dom rising at 9.584ns
  Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
  Clock Uncertainty:    0.000ns

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_22 to SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMC
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X105Y179.CQ    Tcko                  0.198   SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<23>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_22
    SLICE_X104Y178.CX    net (fanout=1)        0.214   SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<22>
    SLICE_X104Y178.CLK   Tdh         (-Th)     0.098   SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<23>
                                                       SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM4_RAMC
    -------------------------------------------------  ---------------------------
    Total                                          0.314ns (0.100ns logic, 0.214ns route)
                                                           (31.8% logic, 68.2% route)

--------------------------------------------------------------------------------
```

```
1491
1492 Paths for end point SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_f⌋
     ↪ ifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM122/SP
     ↪ (SLICE_X90Y164.DX), 1 path
1493 ------------------------------------------------------------------------------
1494 Slack (hold path):      0.361ns (requirement - (clock path skew + uncertainty - data path))
1495   Source:               SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_67 (FF)
1496   Destination:          SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xs⌋
       ↪ t_fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM122/SP
       ↪ (RAM)
1497   Requirement:          0.000ns
1498   Data Path Delay:      0.367ns (Levels of Logic = 0)
1499   Clock Path Skew:      0.006ns (0.072 - 0.066)
1500   Source Clock:         SciEngines_API_Core/cni_dom rising at 9.584ns
1501   Destination Clock:    SciEngines_API_Core/cni_dom rising at 9.584ns
1502   Clock Uncertainty:    0.000ns
1503
1504   Minimum Data Path at Fast Process Corner:
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din_67 to
       ↪ SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generator/⌋
       ↪ gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM122/SP
1505     Location             Delay type         Delay(ns)  Physical Resource
1506                                                        Logical Resource(s)
1507     -------------------------------------------------  -------------------
1508     SLICE_X89Y165.DQ     Tcko                  0.198
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<67>
1509                                                        SciEngines_API_Core/core/channel_up_n⌋
                                                              ↪ ext/lane_in/ff_out_din_67
1510     SLICE_X90Y164.DX     net (fanout=1)        0.250
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/ff_out_din<67>
1511     SLICE_X90Y164.CLK    Tdh         (-Th)     0.081
         ↪ SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_fifo_generato⌋
         ↪ r/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<67>
1512                                                        SciEngines_API_Core/core/channel_up_n⌋
                                                              ↪ ext/lane_in/output_fifo/U0/xst⌋
                                                              ↪ _fifo_generator/gconvfifo.rf/g⌋
                                                              ↪ rf.rf/gntv_or_sync_fifo.mem/gd⌋
                                                              ↪ m.dm/Mram_RAM122/SP
1513     -------------------------------------------------  ---------------------------
1514     Total                                      0.367ns (0.117ns logic, 0.250ns route)
1515                                                        (31.9% logic, 68.1% route)
1516
1517 ------------------------------------------------------------------------------
1518
1519 Component Switching Limit Checks: TS_SciEngines_API_Core_api_clk_mgmt_dn_clkout1 = PERIOD
     ↪ TIMEGRP
1520         "SciEngines_API_Core_api_clk_mgmt_dn_clkout1" TS_CNI_CLK PHASE
```

```
        -0.416666667 ns HIGH 50%;
--------------------------------------------------------------------------------
Slack: 8.270ns (period - min period limit)
  Period: 10.000ns
  Min period limit: 1.730ns (578.035MHz) (Tbcper_I)
  Physical resource: SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf/I0
  Logical resource: SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf/I0
  Location pin: BUFGMUX_X2Y1.I0
  Clock network: SciEngines_API_Core/api_clk_mgmt_dn/clkout1
--------------------------------------------------------------------------------
Slack: 8.962ns (period - min period limit)
  Period: 10.000ns
  Min period limit: 1.038ns (963.391MHz) (Tcp)
  Physical resource: SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_
    ↪ fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<67>/CLK
  Logical resource: SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_f
    ↪ ifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM122/DP/CLK
  Location pin: SLICE_X90Y164.CLK
  Clock network: SciEngines_API_Core/cni_dom
--------------------------------------------------------------------------------
Slack: 8.962ns (period - min period limit)
  Period: 10.000ns
  Min period limit: 1.038ns (963.391MHz) (Tcp)
  Physical resource: SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_
    ↪ fifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/_n0014<67>/CLK
  Logical resource: SciEngines_API_Core/core/channel_up_next/lane_in/output_fifo/U0/xst_f
    ↪ ifo_generator/gconvfifo.rf/grf.rf/gntv_or_sync_fifo.mem/gdm.dm/Mram_RAM122/SP/CLK
  Location pin: SLICE_X90Y164.CLK
  Clock network: SciEngines_API_Core/cni_dom
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TIMEGRP "TNM_CPI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP
"CPI_CLK";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 34 paths analyzed, 17 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   2.666ns.
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[14].cpi_DDR (ILOGIC_X19Y1.D), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     0.334ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<14> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[14].cpi_DDR (FF)
```

```
1563  Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
1564  Requirement:          3.000ns
1565  Data Path Delay:      1.924ns (Levels of Logic = 2)
1566  Clock Path Delay:     -0.064ns (Levels of Logic = 4)
1567  Clock Uncertainty:    0.262ns
1568
1569  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1570    Total System Jitter (TSJ):  0.050ns
1571    Discrete Jitter (DJ):       0.181ns
1572    Phase Error (PE):           0.167ns
1573
1574  Maximum Data Path at Slow Process Corner: CPI<14> to
      ↪  SciEngines_API_Core/lane_phy_con[14].cpi_DDR
1575    Location             Delay type         Delay(ns)  Physical Resource
1576                                                       Logical Resource(s)
1577    -------------------------------------------------  -------------------
1578    AD14.I               Tiopi                 0.790   CPI<14>
1579                                                       CPI<14>
1580                                                    SciEngines_API_Core/lane_phy_con[14].
                                                          ↪  cpi_lane_ibuf
1581                                                       ProtoComp153.IMUX.31
1582    ILOGIC_X19Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<14>
1583    ILOGIC_X19Y1.CLK0    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<29>
1584                                                       ProtoComp163.D2OFFBYP_SRC.31
1585                                                    SciEngines_API_Core/lane_phy_con[14].cpi_DDR
1586    -------------------------------------------------  ---------------------------
1587    Total                                      1.924ns (1.705ns logic, 0.219ns route)
1588                                                       (88.6% logic, 11.4% route)
1589
1590  Minimum Clock Path at Slow Process Corner: CPI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[14].cpi_DDR
1591    Location             Delay type         Delay(ns)  Physical Resource
1592                                                       Logical Resource(s)
1593    -------------------------------------------------  -------------------
1594    AF12.I               Tiopi                 0.684   CPI_CLK
1595                                                       CPI_CLK
1596                                                    SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
1597                                                       ProtoComp162.IMUX.1
1598    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
1599    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
1600                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
1601    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
1602    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
1603                                                    SciEngines_API_Core/api_clk_mgmt_up/p
                                                          ↪  ll_base_inst/PLL_ADV
```

```
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X19Y1.CLK0    net (fanout=1608)     1.409   SciEngines_API_Core/clk_int
    ---------------------------------------------------  ---------------------------
    Total                                      -0.064ns (-2.596ns logic, 2.532ns route)

--------------------------------------------------------------------------------
Slack (setup path):     5.329ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<14> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[14].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.069ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CPI<14> to
    ↪ SciEngines_API_Core/lane_phy_con[14].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    AD14.I               Tiopi                 0.790   CPI<14>
                                                       CPI<14>
                                                  SciEngines_API_Core/lane_phy_con[14].
                                                    ↪ cpi_lane_ibuf
                                                       ProtoComp153.IMUX.31
    ILOGIC_X19Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<14>
    ILOGIC_X19Y1.CLK1    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<29>
                                                       ProtoComp163.D2OFFBYP_SRC.31
                                                SciEngines_API_Core/lane_phy_con[14].cpi_DDR
    ---------------------------------------------------  ---------------------------
    Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[14].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.684   CPI_CLK
                                                         CPI_CLK
                                              SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                         ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                         SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                    SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                      ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X19Y1.CLK1    net (fanout=1608)     1.404   SciEngines_API_Core/clk_int
    ----------------------------------------------------  --------------------------
    Total                                     -0.069ns (-2.596ns logic, 2.527ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[13].cpi_DDR (ILOGIC_X29Y1.D), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     0.339ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<13> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[13].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.059ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CPI<13> to
    ↪ SciEngines_API_Core/lane_phy_con[13].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    Y16.I                Tiopi                 0.790   CPI<13>
                                                        CPI<13>
                                                      SciEngines_API_Core/lane_phy_con[13].
                                                        ↪ cpi_lane_ibuf
                                                        ProtoComp153.IMUX.30
    ILOGIC_X29Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<13>
    ILOGIC_X29Y1.CLK0    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<27>
                                                        ProtoComp163.D2OFFBYP_SRC.30
                                                    SciEngines_API_Core/lane_phy_con[13].cpi_DDR
    ----------------------------------------------------  ---------------------------
    Total                                       1.924ns (1.705ns logic, 0.219ns route)
                                                        (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[13].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ----------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.684   CPI_CLK
                                                        CPI_CLK
                                                  SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                        ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                      SciEngines_API_Core/api_clk_mgmt_up/p
                                                        ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                              SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X29Y1.CLK0    net (fanout=1608)     1.414   SciEngines_API_Core/clk_int
    ----------------------------------------------------  ---------------------------
    Total                                      -0.059ns (-2.596ns logic, 2.537ns route)

--------------------------------------------------------------------------------
Slack (setup path):     5.333ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<13> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[13].cpi_DDR (FF)
```

```
1722  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
1723  Requirement:          3.000ns
1724  Data Path Delay:      1.924ns (Levels of Logic = 2)
1725  Clock Path Delay:     -0.065ns (Levels of Logic = 4)
1726  Clock Uncertainty:    0.262ns
1727
1728  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1729    Total System Jitter (TSJ):  0.050ns
1730    Discrete Jitter (DJ):       0.181ns
1731    Phase Error (PE):           0.167ns
1732
1733  Maximum Data Path at Slow Process Corner: CPI<13> to
      ↪  SciEngines_API_Core/lane_phy_con[13].cpi_DDR
1734    Location             Delay type         Delay(ns)  Physical Resource
1735                                                       Logical Resource(s)
1736    -------------------------------------------------  -------------------
1737    Y16.I                Tiopi                 0.790   CPI<13>
1738                                                       CPI<13>
1739                                                    SciEngines_API_Core/lane_phy_con[13].
                                                          ↪  cpi_lane_ibuf
1740                                                       ProtoComp153.IMUX.30
1741    ILOGIC_X29Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<13>
1742    ILOGIC_X29Y1.CLK1    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<27>
1743                                                       ProtoComp163.D2OFFBYP_SRC.30
1744                                                    SciEngines_API_Core/lane_phy_con[13].cpi_DDR
1745    -------------------------------------------------  ---------------------------
1746    Total                                       1.924ns (1.705ns logic, 0.219ns route)
1747                                                       (88.6% logic, 11.4% route)
1748
1749  Minimum Clock Path at Slow Process Corner: CPI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[13].cpi_DDR
1750    Location             Delay type         Delay(ns)  Physical Resource
1751                                                       Logical Resource(s)
1752    -------------------------------------------------  -------------------
1753    AF12.I               Tiopi                 0.684   CPI_CLK
1754                                                       CPI_CLK
1755                                                    SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
1756                                                       ProtoComp162.IMUX.1
1757    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
1758    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
1759                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
1760    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
1761    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
1762                                                    SciEngines_API_Core/api_clk_mgmt_up/p
                                                          ↪  ll_base_inst/PLL_ADV
```

```
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X29Y1.CLK1    net (fanout=1608)     1.408   SciEngines_API_Core/clk_int
    ---------------------------------------------------  ---------------------------
    Total                                      -0.065ns (-2.596ns logic, 2.531ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[7].cpi_DDR (ILOGIC_X30Y1.D), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     0.340ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<7> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[7].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.058ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CPI<7> to
    ↪ SciEngines_API_Core/lane_phy_con[7].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    V16.I                Tiopi                 0.790   CPI<7>
                                                       CPI<7>
                                          SciEngines_API_Core/lane_phy_con[7].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.17
    ILOGIC_X30Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<7>
    ILOGIC_X30Y1.CLK0    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<15>
                                                       ProtoComp163.D2OFFBYP_SRC.17
                                           SciEngines_API_Core/lane_phy_con[7].cpi_DDR
    ---------------------------------------------------  ---------------------------
    Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[7].cpi_DDR
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.684   CPI_CLK
                                                       CPI_CLK
                                            SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                    SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                      ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X30Y1.CLK0    net (fanout=1608)     1.415   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
    Total                                     -0.058ns (-2.596ns logic, 2.538ns route)

--------------------------------------------------------------------------------
Slack (setup path):     5.335ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CPI<7> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[7].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.063ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CPI<7> to
    ↪ SciEngines_API_Core/lane_phy_con[7].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    V16.I                Tiopi                 0.790   CPI<7>
                                                       CPI<7>
                                          SciEngines_API_Core/lane_phy_con[7].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.17
    ILOGIC_X30Y1.D       net (fanout=1)        0.219   SciEngines_API_Core/cpiLane_rx<7>
    ILOGIC_X30Y1.CLK1    Tidock                0.915   SciEngines_API_Core/cpiLane_fd0<15>
                                                       ProtoComp163.D2OFFBYP_SRC.17
                                           SciEngines_API_Core/lane_phy_con[7].cpi_DDR
    ------------------------------------------------  --------------------------
    Total                                     1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[7].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.684   CPI_CLK
                                                       CPI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -3.582
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                 SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                    ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.391
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X30Y1.CLK1    net (fanout=1608)     1.410   SciEngines_API_Core/clk_int
    ------------------------------------------------  --------------------------
    Total                                    -0.063ns (-2.596ns logic, 2.533ns route)

--------------------------------------------------------------------------------

Hold Paths: TIMEGRP "TNM_CPI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP "CPI_CLK";
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[0].cpi_DDR (ILOGIC_X11Y2.D), 2 paths
--------------------------------------------------------------------------------
```

```
Slack (hold path):      2.652ns (requirement - (clock path + clock arrival + uncertainty - data path))
  Source:               CPI<0> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[0].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
  Requirement:          6.400ns
  Data Path Delay:      0.917ns (Levels of Logic = 2)
  Clock Path Delay:     -0.181ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CPI<0> to SciEngines_API_Core/lane_phy_con[0].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AD11.I               Tiopi                 0.321   CPI<0>
                                                       CPI<0>
                                          SciEngines_API_Core/lane_phy_con[0].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.10
    ILOGIC_X11Y2.D       net (fanout=1)        0.095   SciEngines_API_Core/cpiLane_rx<0>
    ILOGIC_X11Y2.CLK1    Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<1>
                                                       ProtoComp163.D2OFFBYP_SRC.10
                                           SciEngines_API_Core/lane_phy_con[0].cpi_DDR
    -------------------------------------------------  ---------------------------
    Total                                     0.917ns (0.822ns logic, 0.095ns route)
                                                       (89.6% logic, 10.4% route)

  Maximum Clock Path at Fast Process Corner: CPI_CLK to SciEngines_API_Core/lane_phy_con[0].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.367   CPI_CLK
                                                       CPI_CLK
                                        SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.213
      SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
      SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
```

```
1926    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
        ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
1927                                                  SciEngines_API_Core/api_clk_mgmt_up/p┘
                                                         ↪ ll_base_inst/PLL_ADV
1928    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
1929    BUFGMUX_X2Y4.O       Tgi0o                 0.063
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
1930                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
1931    ILOGIC_X11Y2.CLK1    net (fanout=1608)     1.039   SciEngines_API_Core/clk_int
1932    ---------------------------------------------------  ---------------------------
1933    Total                                       -0.181ns (-1.917ns logic, 1.736ns route)
1934
1935 --------------------------------------------------------------------------------
1936 Slack (hold path):      7.577ns (requirement - (clock path + clock arrival + uncertainty -
    ↪ data path))
1937   Source:               CPI<0> (PAD)
1938   Destination:          SciEngines_API_Core/lane_phy_con[0].cpi_DDR (FF)
1939   Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
1940   Requirement:          6.400ns
1941   Data Path Delay:      0.917ns (Levels of Logic = 2)
1942   Clock Path Delay:     -0.106ns (Levels of Logic = 4)
1943   Clock Uncertainty:    0.262ns
1944
1945   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
1946     Total System Jitter (TSJ):  0.050ns
1947     Discrete Jitter (DJ):       0.181ns
1948     Phase Error (PE):           0.167ns
1949
1950   Minimum Data Path at Fast Process Corner: CPI<0> to
       ↪ SciEngines_API_Core/lane_phy_con[0].cpi_DDR
1951     Location             Delay type         Delay(ns)  Physical Resource
1952                                                        Logical Resource(s)
1953     ---------------------------------------------------  -------------------
1954     AD11.I               Tiopi                 0.321   CPI<0>
1955                                                        CPI<0>
1956                                          SciEngines_API_Core/lane_phy_con[0].cpi_lane_ibuf
1957                                                        ProtoComp153.IMUX.10
1958     ILOGIC_X11Y2.D       net (fanout=1)        0.095   SciEngines_API_Core/cpiLane_rx<0>
1959     ILOGIC_X11Y2.CLK0    Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<1>
1960                                                        ProtoComp163.D2OFFBYP_SRC.10
1961                                                 SciEngines_API_Core/lane_phy_con[0].cpi_DDR
1962     ---------------------------------------------------  ---------------------------
1963     Total                                       0.917ns (0.822ns logic, 0.095ns route)
1964                                                        (89.6% logic, 10.4% route)
1965
1966   Maximum Clock Path at Fast Process Corner: CPI_CLK to
       ↪ SciEngines_API_Core/lane_phy_con[0].cpi_DDR
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.367   CPI_CLK
                                                       CPI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.213
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                     SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                       ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X11Y2.CLK0    net (fanout=1608)     1.114   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
    Total                                     -0.106ns (-1.917ns logic, 1.811ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[5].cpi_DDR (ILOGIC_X17Y2.D), 2 paths
--------------------------------------------------------------------------------
Slack (hold path):      2.655ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CPI<5> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[5].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
  Requirement:          6.400ns
  Data Path Delay:      0.917ns (Levels of Logic = 2)
  Clock Path Delay:     -0.184ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CPI<5> to
    ↪ SciEngines_API_Core/lane_phy_con[5].cpi_DDR
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AB13.I               Tiopi                 0.321   CPI<5>
                                                       CPI<5>
                                          SciEngines_API_Core/lane_phy_con[5].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.15
    ILOGIC_X17Y2.D       net (fanout=1)        0.095   SciEngines_API_Core/cpiLane_rx<5>
    ILOGIC_X17Y2.CLK1    Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<11>
                                                       ProtoComp163.D2OFFBYP_SRC.15
                                           SciEngines_API_Core/lane_phy_con[5].cpi_DDR
    -------------------------------------------------  ---------------------------
    Total                                     0.917ns (0.822ns logic, 0.095ns route)
                                                       (89.6% logic, 10.4% route)

  Maximum Clock Path at Fast Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[5].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.367   CPI_CLK
                                                       CPI_CLK
                                          SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.213
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                  ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X17Y2.CLK1    net (fanout=1608)     1.036   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
    Total                                    -0.184ns (-1.917ns logic, 1.733ns route)

--------------------------------------------------------------------------------
Slack (hold path):      7.581ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CPI<5> (PAD)
```

```
Destination:          SciEngines_API_Core/lane_phy_con[5].cpi_DDR (FF)
Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
Requirement:          6.400ns
Data Path Delay:      0.917ns (Levels of Logic = 2)
Clock Path Delay:     -0.110ns (Levels of Logic = 4)
Clock Uncertainty:    0.262ns

Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Minimum Data Path at Fast Process Corner: CPI<5> to
  ↪ SciEngines_API_Core/lane_phy_con[5].cpi_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  AB13.I               Tiopi                 0.321   CPI<5>
                                                     CPI<5>
                                       SciEngines_API_Core/lane_phy_con[5].cpi_lane_ibuf
                                                     ProtoComp153.IMUX.15
  ILOGIC_X17Y2.D       net (fanout=1)        0.095   SciEngines_API_Core/cpiLane_rx<5>
  ILOGIC_X17Y2.CLK0    Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<11>
                                                     ProtoComp163.D2OFFBYP_SRC.15
                                        SciEngines_API_Core/lane_phy_con[5].cpi_DDR
  -------------------------------------------------  ---------------------------
  Total                                      0.917ns (0.822ns logic, 0.095ns route)
                                                     (89.6% logic, 10.4% route)

Maximum Clock Path at Fast Process Corner: CPI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[5].cpi_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  AF12.I               Tiopi                 0.367   CPI_CLK
                                                     CPI_CLK
                                      SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                     ProtoComp162.IMUX.1
  BUFIO2_X1Y7.I        net (fanout=1)        0.213
    ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
  BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
  PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
    ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
    ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                           SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                             ↪ ll_base_inst/PLL_ADV
```

```
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X17Y2.CLK0    net (fanout=1608)     1.110   SciEngines_API_Core/clk_int
    ---------------------------------------------------  ---------------------------
    Total                                      -0.110ns (-1.917ns logic, 1.807ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[1].cpi_DDR (ILOGIC_X8Y3.D), 2 paths
--------------------------------------------------------------------------------
Slack (hold path):      2.681ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CPI<1> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[1].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int falling at 4.584ns
  Requirement:          6.400ns
  Data Path Delay:      0.946ns (Levels of Logic = 2)
  Clock Path Delay:     -0.181ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CPI<1> to
    ↪ SciEngines_API_Core/lane_phy_con[1].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    Y10.I                Tiopi                 0.321   CPI<1>
                                                       CPI<1>
                                          SciEngines_API_Core/lane_phy_con[1].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.11
    ILOGIC_X8Y3.D        net (fanout=1)        0.124   SciEngines_API_Core/cpiLane_rx<1>
    ILOGIC_X8Y3.CLK1     Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<3>
                                                       ProtoComp163.D2OFFBYP_SRC.11
                                           SciEngines_API_Core/lane_phy_con[1].cpi_DDR
    ---------------------------------------------------  ---------------------------
    Total                                      0.946ns (0.822ns logic, 0.124ns route)
                                                       (86.9% logic, 13.1% route)

  Maximum Clock Path at Fast Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[1].cpi_DDR
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.367   CPI_CLK
                                                       CPI_CLK
                                            SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.213
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                    SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                      ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X8Y3.CLK1     net (fanout=1608)     1.039   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
    Total                                     -0.181ns (-1.917ns logic, 1.736ns route)

--------------------------------------------------------------------------------
Slack (hold path):      7.606ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CPI<1> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[1].cpi_DDR (FF)
  Destination Clock:    SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          6.400ns
  Data Path Delay:      0.946ns (Levels of Logic = 2)
  Clock Path Delay:     -0.106ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CPI<1> to
    ↪ SciEngines_API_Core/lane_phy_con[1].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
```

```
    Y10.I                Tiopi                 0.321   CPI<1>
                                                       CPI<1>
                                          SciEngines_API_Core/lane_phy_con[1].cpi_lane_ibuf
                                                       ProtoComp153.IMUX.11
    ILOGIC_X8Y3.D        net (fanout=1)        0.124   SciEngines_API_Core/cpiLane_rx<1>
    ILOGIC_X8Y3.CLK0     Tiockd      (-Th)    -0.501   SciEngines_API_Core/cpiLane_fd0<3>
                                                       ProtoComp163.D2OFFBYP_SRC.11
                                           SciEngines_API_Core/lane_phy_con[1].cpi_DDR
    ---------------------------------------------------  ---------------------------
    Total                                     0.946ns (0.822ns logic, 0.124ns route)
                                                       (86.9% logic, 13.1% route)

  Maximum Clock Path at Fast Process Corner: CPI_CLK to
    ↪  SciEngines_API_Core/lane_phy_con[1].cpi_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.367   CPI_CLK
                                                       CPI_CLK
                                         SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.213
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.339
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.477
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                   ↪  ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.145
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.063
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    ILOGIC_X8Y3.CLK0     net (fanout=1608)     1.114   SciEngines_API_Core/clk_int
    ---------------------------------------------------  ---------------------------
    Total                                    -0.106ns (-1.917ns logic, 1.811ns route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: TIMEGRP "TNM_CPO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 17 paths analyzed, 17 endpoints analyzed, 0 failing endpoints
```

```
 0 timing errors detected.
 Minimum allowable offset is   2.364ns.
--------------------------------------------------------------------------------

Paths for end point CPO<14> (AB10.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  0.566ns (requirement - (clock arrival + clock path + data path + uncertainty))
  Source:               SciEngines_API_Core/lane_phy_con[14].cpo_DDR (FF)
  Destination:          CPO<14> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          2.930ns
  Data Path Delay:      3.575ns (Levels of Logic = 1)
  Clock Path Delay:     -1.057ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Clock Path at Slow Process Corner: CPI_CLK to SciEngines_API_Core/lane_phy_con[14].cpo_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.790   CPI_CLK
                                                       CPI_CLK
                                            SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.396
      SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
      SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
      SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
      SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.209
      SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                            SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    OLOGIC_X8Y2.CLK0     net (fanout=1608)     1.911   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
```

```
2247    Total                                     -1.057ns (-4.352ns logic, 3.295ns route)
2248
2249  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[14].cpo_DDR to
      ↪ CPO<14>
2250    Location             Delay type         Delay(ns)  Physical Resource
2251                                                       Logical Resource(s)
2252    -------------------------------------------------  -------------------
2253    OLOGIC_X8Y2.OQ       Tockq                 0.742   SciEngines_API_Core/cpoLane_tx<14>
2254                                                       SciEngines_API_Core/lane_phy_con[14].cpo_DDR
2255    AB10.O               net (fanout=1)        0.362   SciEngines_API_Core/cpoLane_tx<14>
2256    AB10.PAD             Tioop                 2.471   CPO<14>
2257                                                       SciEngines_API_Core/lane_phy_con[14].┘
                                                             ↪ cpo_lane_obuf
2258                                                       CPO<14>
2259    -------------------------------------------------  ---------------------------
2260    Total                                     3.575ns (3.213ns logic, 0.362ns route)
2261                                                       (89.9% logic, 10.1% route)
2262
2263 --------------------------------------------------------------------------------
2264
2265 Paths for end point CPO<6> (AC11.PAD), 1 path
2266 --------------------------------------------------------------------------------
2267 Slack (slowest paths):  0.567ns (requirement - (clock arrival + clock path + data path +
    ↪ uncertainty))
2268   Source:               SciEngines_API_Core/lane_phy_con[6].cpo_DDR (FF)
2269   Destination:          CPO<6> (PAD)
2270   Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
2271   Requirement:          2.930ns
2272   Data Path Delay:      3.575ns (Levels of Logic = 1)
2273   Clock Path Delay:     -1.058ns (Levels of Logic = 4)
2274   Clock Uncertainty:    0.262ns
2275
2276   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
2277     Total System Jitter (TSJ):  0.050ns
2278     Discrete Jitter (DJ):       0.181ns
2279     Phase Error (PE):           0.167ns
2280
2281   Maximum Clock Path at Slow Process Corner: CPI_CLK to
      ↪ SciEngines_API_Core/lane_phy_con[6].cpo_DDR
2282     Location             Delay type         Delay(ns)  Physical Resource
2283                                                        Logical Resource(s)
2284     -------------------------------------------------  -------------------
2285     AF12.I               Tiopi                 0.790   CPI_CLK
2286                                                        CPI_CLK
2287                                                      SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
2288                                                        ProtoComp162.IMUX.1
2289     BUFIO2_X1Y7.I        net (fanout=1)        0.396
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
```

```
2290    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2291                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2292    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
        ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2293    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
        ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
2294                                                    SciEngines_API_Core/api_clk_mgmt_up/p
                                                           ↪ ll_base_inst/PLL_ADV
2295    BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
2296    BUFGMUX_X2Y4.O       Tgi0o                 0.209
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2297                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2298    OLOGIC_X11Y3.CLK0    net (fanout=1608)     1.910   SciEngines_API_Core/clk_int
2299    ---------------------------------------------------  ---------------------------
2300    Total                                      -1.058ns (-4.352ns logic, 3.294ns route)
2301
2302  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[6].cpo_DDR to
      ↪ CPO<6>
2303    Location             Delay type         Delay(ns)  Physical Resource
2304                                                       Logical Resource(s)
2305    ---------------------------------------------------  -------------------
2306    OLOGIC_X11Y3.OQ      Tockq                 0.742   SciEngines_API_Core/cpoLane_tx<6>
2307                                                        SciEngines_API_Core/lane_phy_con[6].cpo_DDR
2308    AC11.O               net (fanout=1)        0.362   SciEngines_API_Core/cpoLane_tx<6>
2309    AC11.PAD             Tioop                 2.471   CPO<6>
2310                                         SciEngines_API_Core/lane_phy_con[6].cpo_lane_obuf
2311                                                       CPO<6>
2312    ---------------------------------------------------  ---------------------------
2313    Total                                      3.575ns (3.213ns logic, 0.362ns route)
2314                                                       (89.9% logic, 10.1% route)
2315
2316 --------------------------------------------------------------------------------
2317
2318 Paths for end point CPO<10> (AE11.PAD), 1 path
2319 --------------------------------------------------------------------------------
2320 Slack (slowest paths):  0.568ns (requirement - (clock arrival + clock path + data path +
      ↪ uncertainty))
2321   Source:               SciEngines_API_Core/lane_phy_con[10].cpo_DDR (FF)
2322   Destination:          CPO<10> (PAD)
2323   Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
2324   Requirement:          2.930ns
2325   Data Path Delay:      3.575ns (Levels of Logic = 1)
2326   Clock Path Delay:     -1.059ns (Levels of Logic = 4)
2327   Clock Uncertainty:    0.262ns
2328
2329   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
```

```
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Maximum Clock Path at Slow Process Corner: CPI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[10].cpo_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  ---------------------------------------------------  -------------------
  AF12.I               Tiopi                 0.790   CPI_CLK
                                                     CPI_CLK
                                          SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                     ProtoComp162.IMUX.1
  BUFIO2_X1Y7.I        net (fanout=1)        0.396
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
  BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
  PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
  ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
  ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                  ↪ ll_base_inst/PLL_ADV
  BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
  BUFGMUX_X2Y4.O       Tgi0o                 0.209
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
  OLOGIC_X10Y3.CLK0    net (fanout=1608)     1.909   SciEngines_API_Core/clk_int
  ---------------------------------------------------  ---------------------------
  Total                                     -1.059ns (-4.352ns logic, 3.293ns route)

Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[10].cpo_DDR to
  ↪ CPO<10>
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  ---------------------------------------------------  -------------------
  OLOGIC_X10Y3.OQ      Tockq                 0.742   SciEngines_API_Core/cpoLane_tx<10>
                                          SciEngines_API_Core/lane_phy_con[10].cpo_DDR
  AE11.O               net (fanout=1)        0.362   SciEngines_API_Core/cpoLane_tx<10>
  AE11.PAD             Tioop                 2.471   CPO<10>
                                                SciEngines_API_Core/lane_phy_con[10].⌋
                                                  ↪ cpo_lane_obuf
                                                     CPO<10>
  ---------------------------------------------------  ---------------------------
  Total                                     3.575ns (3.213ns logic, 0.362ns route)
                                                     (89.9% logic, 10.1% route)
```

```
2368
2369 --------------------------------------------------------------------------------
2370
2371 Fastest Paths: TIMEGRP "TNM_CPO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
2372 --------------------------------------------------------------------------------
2373
2374 Paths for end point CPO<13> (Y18.PAD), 1 path
2375 --------------------------------------------------------------------------------
2376 Delay (fastest paths):  1.093ns (clock arrival + clock path + data path - uncertainty)
2377   Source:               SciEngines_API_Core/lane_phy_con[13].cpo_DDR (FF)
2378   Destination:          CPO<13> (PAD)
2379   Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
2380   Data Path Delay:      2.168ns (Levels of Logic = 1)
2381   Clock Path Delay:     -0.397ns (Levels of Logic = 4)
2382   Clock Uncertainty:    0.262ns
2383
2384   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
2385     Total System Jitter (TSJ):  0.050ns
2386     Discrete Jitter (DJ):       0.181ns
2387     Phase Error (PE):           0.167ns
2388
2389   Minimum Clock Path at Fast Process Corner: CPI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[13].cpo_DDR
2390     Location             Delay type         Delay(ns)  Physical Resource
2391                                                        Logical Resource(s)
2392     -------------------------------------------------  -------------------
2393     AF12.I               Tiopi                 0.321   CPI_CLK
2394                                                        CPI_CLK
2395                                             SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
2396                                                        ProtoComp162.IMUX.1
2397     BUFIO2_X1Y7.I        net (fanout=1)        0.203
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
2398     BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2399                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2400     PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2401     PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
2402                                                   SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                         ↪  ll_base_inst/PLL_ADV
2403     BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout0
2404     BUFGMUX_X2Y4.O       Tgi0o                 0.059
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2405                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2406     OLOGIC_X31Y1.CLK0    net (fanout=1608)     0.752   SciEngines_API_Core/clk_int
2407     -------------------------------------------------  ---------------------------
```

```
    Total                                     -0.397ns (-1.786ns logic, 1.389ns route)

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[13].cpo_DDR to
    ↪ CPO<13>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    OLOGIC_X31Y1.OQ      Tockq                 0.419   SciEngines_API_Core/cpoLane_tx<13>
                                                      SciEngines_API_Core/lane_phy_con[13].cpo_DDR
    Y18.O                net (fanout=1)        0.268   SciEngines_API_Core/cpoLane_tx<13>
    Y18.PAD              Tioop                 1.481   CPO<13>
                                                           SciEngines_API_Core/lane_phy_con[13].┘
                                                             ↪ cpo_lane_obuf
                                                       CPO<13>
    -------------------------------------------------  ---------------------------
    Total                                     2.168ns (1.900ns logic, 0.268ns route)
                                                       (87.6% logic, 12.4% route)

--------------------------------------------------------------------------------

Paths for end point CPO<3> (AA14.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  1.135ns (clock arrival + clock path + data path - uncertainty)
  Source:               SciEngines_API_Core/lane_phy_con[3].cpo_DDR (FF)
  Destination:          CPO<3> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Data Path Delay:      2.219ns (Levels of Logic = 1)
  Clock Path Delay:     -0.406ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Clock Path at Fast Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[3].cpo_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.321   CPI_CLK
                                                       CPI_CLK
                                                    SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.203
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
```

```
                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
      ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                      SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                         ↪  ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.059
      ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    OLOGIC_X20Y2.CLK0    net (fanout=1608)     0.743   SciEngines_API_Core/clk_int
    ---------------------------------------------------  ---------------------------
    Total                                     -0.406ns (-1.786ns logic, 1.380ns route)

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[3].cpo_DDR to
    ↪  CPO<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    OLOGIC_X20Y2.OQ      Tockq                 0.419   SciEngines_API_Core/cpoLane_tx<3>
                                                        SciEngines_API_Core/lane_phy_con[3].cpo_DDR
    AA14.O               net (fanout=1)        0.319   SciEngines_API_Core/cpoLane_tx<3>
    AA14.PAD             Tioop                 1.481   CPO<3>
                                          SciEngines_API_Core/lane_phy_con[3].cpo_lane_obuf
                                                       CPO<3>
    ---------------------------------------------------  ---------------------------
    Total                                     2.219ns (1.900ns logic, 0.319ns route)
                                                       (85.6% logic, 14.4% route)

--------------------------------------------------------------------------------

Paths for end point CPO<5> (AD18.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  1.141ns (clock arrival + clock path + data path - uncertainty)
  Source:               SciEngines_API_Core/lane_phy_con[5].cpo_DDR (FF)
  Destination:          CPO<5> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Data Path Delay:      2.219ns (Levels of Logic = 1)
  Clock Path Delay:     -0.400ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns
```

```
2492
2493  Minimum Clock Path at Fast Process Corner: CPI_CLK to
      ↪ SciEngines_API_Core/lane_phy_con[5].cpo_DDR
2494    Location             Delay type         Delay(ns)  Physical Resource
2495                                                       Logical Resource(s)
2496    -------------------------------------------------  -------------------
2497    AF12.I               Tiopi                 0.321   CPI_CLK
2498                                                       CPI_CLK
2499                                           SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
2500                                                       ProtoComp162.IMUX.1
2501    BUFIO2_X1Y7.I        net (fanout=1)        0.203
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
2502    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2503                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
2504    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
        ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2505    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
        ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
2506                                                   SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                          ↪ ll_base_inst/PLL_ADV
2507    BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
2508    BUFGMUX_X2Y4.O       Tgi0o                 0.059
        ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2509                                         SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
2510    OLOGIC_X30Y3.CLK0    net (fanout=1608)     0.749   SciEngines_API_Core/clk_int
2511    -------------------------------------------------  ---------------------------
2512    Total                                     -0.400ns (-1.786ns logic, 1.386ns route)
2513
2514  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[5].cpo_DDR to
      ↪ CPO<5>
2515    Location             Delay type         Delay(ns)  Physical Resource
2516                                                       Logical Resource(s)
2517    -------------------------------------------------  -------------------
2518    OLOGIC_X30Y3.OQ      Tockq                 0.419   SciEngines_API_Core/cpoLane_tx<5>
2519                                           SciEngines_API_Core/lane_phy_con[5].cpo_DDR
2520    AD18.O               net (fanout=1)        0.319   SciEngines_API_Core/cpoLane_tx<5>
2521    AD18.PAD             Tioop                 1.481   CPO<5>
2522                                         SciEngines_API_Core/lane_phy_con[5].cpo_lane_obuf
2523                                                       CPO<5>
2524    -------------------------------------------------  ---------------------------
2525    Total                                     2.219ns (1.900ns logic, 0.319ns route)
2526                                                       (85.6% logic, 14.4% route)
2527
2528 --------------------------------------------------------------------------------
2529
2530 ================================================================================
```

```
Timing constraint: TIMEGRP "TNM_CNI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP
"CNI_CLK";
For more information, see Offset In Analysis in the Timing Closure User Guide (UG612).

 34 paths analyzed, 17 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum allowable offset is   2.656ns.
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[14].cni_DDR (ILOGIC_X28Y175.D), 2
  ↪ paths
--------------------------------------------------------------------------------
Slack (setup path):     0.344ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CNI<14> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[14].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.054ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CNI<14> to
    ↪ SciEngines_API_Core/lane_phy_con[14].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    K15.I                Tiopi                 0.790   CNI<14>
                                                       CNI<14>
                                                    SciEngines_API_Core/lane_phy_con[14].┘
                                                      ↪ cni_lane_ibuf
                                                       ProtoComp153.IMUX.24
    ILOGIC_X28Y175.D     net (fanout=1)        0.219   SciEngines_API_Core/cniLane_rx<14>
    ILOGIC_X28Y175.CLK0  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<29>
                                                       ProtoComp163.D2OFFBYP_SRC.24
                                                    SciEngines_API_Core/lane_phy_con[14].cni_DDR
    -------------------------------------------------  ---------------------------
    Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[14].cni_DDR
```

```
2573    Location             Delay type         Delay(ns)  Physical Resource
2574                                                       Logical Resource(s)
2575    -------------------------------------------------  -------------------
2576    B14.I                Tiopi                 0.684   CNI_CLK
2577                                                       CNI_CLK
2578                                              SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
2579                                                       ProtoComp162.IMUX
2580    BUFIO2_X2Y26.I       net (fanout=1)        0.246
        ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
2581    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2582                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2583    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
        ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2584    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
        ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
2585                                                    SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                          ↪ ll_base_inst/PLL_ADV
2586    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488
        ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
2587    BUFGMUX_X2Y1.O       Tgi0o                 0.197
        ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2588                                            SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2589    ILOGIC_X28Y175.CLK0  net (fanout=241)      1.413   SciEngines_API_Core/cni_dom
2590    -------------------------------------------------  ---------------------------
2591    Total                                     -0.054ns (-2.687ns logic, 2.633ns route)
2592
2593 --------------------------------------------------------------------------------
2594 Slack (setup path):     5.338ns (requirement - (data path - clock path - clock arrival +
    ↪ uncertainty))
2595   Source:               CNI<14> (PAD)
2596   Destination:          SciEngines_API_Core/lane_phy_con[14].cni_DDR (FF)
2597   Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
2598   Requirement:          3.000ns
2599   Data Path Delay:      1.924ns (Levels of Logic = 2)
2600   Clock Path Delay:     -0.060ns (Levels of Logic = 4)
2601   Clock Uncertainty:    0.262ns
2602
2603   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
2604     Total System Jitter (TSJ):  0.050ns
2605     Discrete Jitter (DJ):       0.181ns
2606     Phase Error (PE):           0.167ns
2607
2608   Maximum Data Path at Slow Process Corner: CNI<14> to
       ↪ SciEngines_API_Core/lane_phy_con[14].cni_DDR
2609     Location             Delay type         Delay(ns)  Physical Resource
2610                                                       Logical Resource(s)
2611     -------------------------------------------------  -------------------
```

```
    K15.I                Tiopi                 0.790   CNI<14>
                                                       CNI<14>
                                                     SciEngines_API_Core/lane_phy_con[14].
                                                       ↪ cni_lane_ibuf
                                                       ProtoComp153.IMUX.24
    ILOGIC_X28Y175.D     net (fanout=1)        0.219   SciEngines_API_Core/cniLane_rx<14>
    ILOGIC_X28Y175.CLK1  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<29>
                                                       ProtoComp163.D2OFFBYP_SRC.24
                                                   SciEngines_API_Core/lane_phy_con[14].cni_DDR
    -------------------------------------------------  ---------------------------
    Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[14].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    B14.I                Tiopi                 0.684   CNI_CLK
                                                       CNI_CLK
                                              SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                       ProtoComp162.IMUX
    BUFIO2_X2Y26.I       net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                     SciEngines_API_Core/api_clk_mgmt_dn/p
                                                       ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                            SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X28Y175.CLK1  net (fanout=241)      1.407   SciEngines_API_Core/cni_dom
    -------------------------------------------------  ---------------------------
    Total                                     -0.060ns (-2.687ns logic, 2.627ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[6].cni_DDR (ILOGIC_X27Y175.D), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     0.345ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
```

```
Source:               CNI<6> (PAD)
Destination:          SciEngines_API_Core/lane_phy_con[6].cni_DDR (FF)
Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
Requirement:          3.000ns
Data Path Delay:      1.924ns (Levels of Logic = 2)
Clock Path Delay:     -0.053ns (Levels of Logic = 4)
Clock Uncertainty:    0.262ns

Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Maximum Data Path at Slow Process Corner: CNI<6> to
  ↪ SciEngines_API_Core/lane_phy_con[6].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  J15.I                Tiopi                 0.790   CNI<6>
                                                     CNI<6>
                                          SciEngines_API_Core/lane_phy_con[6].cni_lane_ibuf
                                                     ProtoComp153.IMUX.6
  ILOGIC_X27Y175.D     net (fanout=1)        0.219   SciEngines_API_Core/cniLane_rx<6>
  ILOGIC_X27Y175.CLK0  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<13>
                                                     ProtoComp163.D2OFFBYP_SRC.6
                                           SciEngines_API_Core/lane_phy_con[6].cni_DDR
  -------------------------------------------------  ---------------------------
  Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                     (88.6% logic, 11.4% route)

Minimum Clock Path at Slow Process Corner: CNI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[6].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  B14.I                Tiopi                 0.684   CNI_CLK
                                                     CNI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                     ProtoComp162.IMUX
  BUFIO2_X2Y26.I       net (fanout=1)        0.246
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
  BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
  PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
```

```
                                                        SciEngines_API_Core/api_clk_mgmt_dn/p
                                                          ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                          SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X27Y175.CLK0  net (fanout=241)      1.414   SciEngines_API_Core/cni_dom
    ------------------------------------------------  --------------------------
    Total                                     -0.053ns (-2.687ns logic, 2.634ns route)

--------------------------------------------------------------------------------
Slack (setup path):     5.339ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CNI<6> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[6].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
  Requirement:          3.000ns
  Data Path Delay:      1.924ns (Levels of Logic = 2)
  Clock Path Delay:     -0.059ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CNI<6> to
    ↪ SciEngines_API_Core/lane_phy_con[6].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    J15.I                Tiopi                 0.790   CNI<6>
                                                       CNI<6>
                                        SciEngines_API_Core/lane_phy_con[6].cni_lane_ibuf
                                                       ProtoComp153.IMUX.6
    ILOGIC_X27Y175.D     net (fanout=1)        0.219   SciEngines_API_Core/cniLane_rx<6>
    ILOGIC_X27Y175.CLK1  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<13>
                                                       ProtoComp163.D2OFFBYP_SRC.6
                                         SciEngines_API_Core/lane_phy_con[6].cni_DDR
    -------------------------------------------------  -------------------------
    Total                                      1.924ns (1.705ns logic, 0.219ns route)
                                                       (88.6% logic, 11.4% route)

  Minimum Clock Path at Slow Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[6].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                        Logical Resource(s)
    ------------------------------------------------  -------------------
    B14.I                Tiopi                 0.684   CNI_CLK
                                                        CNI_CLK
                                              SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                        ProtoComp162.IMUX
    BUFIO2_X2Y26.I       net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                    SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                      ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                            SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X27Y175.CLK1  net (fanout=241)      1.408   SciEngines_API_Core/cni_dom
    ------------------------------------------------  --------------------------
    Total                                     -0.059ns (-2.687ns logic, 2.628ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[2].cni_DDR (ILOGIC_X24Y174.D), 2 paths
--------------------------------------------------------------------------------
Slack (setup path):     0.389ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CNI<2> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[2].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
  Requirement:          3.000ns
  Data Path Delay:      1.876ns (Levels of Logic = 2)
  Clock Path Delay:     -0.057ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Data Path at Slow Process Corner: CNI<2> to
    ↪ SciEngines_API_Core/lane_phy_con[2].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                    Logical Resource(s)
    ------------------------------------------------  -------------------
    K14.I                Tiopi                 0.790   CNI<2>
                                                    CNI<2>
                                          SciEngines_API_Core/lane_phy_con[2].cni_lane_ibuf
                                                    ProtoComp153.IMUX.2
    ILOGIC_X24Y174.D     net (fanout=1)        0.171   SciEngines_API_Core/cniLane_rx<2>
    ILOGIC_X24Y174.CLK0  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<5>
                                                    ProtoComp163.D2OFFBYP_SRC.2
                                           SciEngines_API_Core/lane_phy_con[2].cni_DDR
    ------------------------------------------------  --------------------------
    Total                                      1.876ns (1.705ns logic, 0.171ns route)
                                                    (90.9% logic, 9.1% route)

  Minimum Clock Path at Slow Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[2].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
    ------------------------------------------------  -------------------
    B14.I                Tiopi                 0.684   CNI_CLK
                                                    CNI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                    ProtoComp162.IMUX
    BUFIO2_X2Y26.I       net (fanout=1)        0.246
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                    SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                  SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                    ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.197
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X24Y174.CLK0  net (fanout=241)      1.410   SciEngines_API_Core/cni_dom
    ------------------------------------------------  --------------------------
    Total                                     -0.057ns (-2.687ns logic, 2.630ns route)

--------------------------------------------------------------------------------
Slack (setup path):     5.384ns (requirement - (data path - clock path - clock arrival +
  ↪ uncertainty))
  Source:               CNI<2> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[2].cni_DDR (FF)
```

```
Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
Requirement:          3.000ns
Data Path Delay:      1.876ns (Levels of Logic = 2)
Clock Path Delay:     -0.062ns (Levels of Logic = 4)
Clock Uncertainty:    0.262ns

Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Maximum Data Path at Slow Process Corner: CNI<2> to
  ↪ SciEngines_API_Core/lane_phy_con[2].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  K14.I                Tiopi                 0.790   CNI<2>
                                                     CNI<2>
                                          SciEngines_API_Core/lane_phy_con[2].cni_lane_ibuf
                                                     ProtoComp153.IMUX.2
  ILOGIC_X24Y174.D     net (fanout=1)        0.171   SciEngines_API_Core/cniLane_rx<2>
  ILOGIC_X24Y174.CLK1  Tidock                0.915   SciEngines_API_Core/cniLane_fd0<5>
                                                     ProtoComp163.D2OFFBYP_SRC.2
                                           SciEngines_API_Core/lane_phy_con[2].cni_DDR
  -------------------------------------------------  ---------------------------
  Total                                      1.876ns (1.705ns logic, 0.171ns route)
                                                     (90.9% logic, 9.1% route)

Minimum Clock Path at Slow Process Corner: CNI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[2].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  B14.I                Tiopi                 0.684   CNI_CLK
                                                     CNI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                     ProtoComp162.IMUX
  BUFIO2_X2Y26.I       net (fanout=1)        0.246
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
  BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.105   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
  PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.486
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -3.673
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                SciEngines_API_Core/api_clk_mgmt_dn/p
                                                  ↪ ll_base_inst/PLL_ADV
```

```
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.488   SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.197   SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                                       SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X24Y174.CLK1  net (fanout=241)      1.405   SciEngines_API_Core/cni_dom
    ------------------------------------------------  ---------------------------
    Total                                     -0.062ns (-2.687ns logic, 2.625ns route)

--------------------------------------------------------------------------------

Hold Paths: TIMEGRP "TNM_CNI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP "CNI_CLK";
--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[10].cni_DDR (ILOGIC_X16Y173.D), 2 paths
--------------------------------------------------------------------------------
Slack (hold path):      2.609ns (requirement - (clock path + clock arrival + uncertainty - data path))
  Source:               CNI<10> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[10].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
  Requirement:          6.400ns
  Data Path Delay:      0.946ns (Levels of Logic = 2)
  Clock Path Delay:     -0.109ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CNI<10> to SciEngines_API_Core/lane_phy_con[10].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D12.I                Tiopi                 0.321   CNI<10>
                                                       CNI<10>
                                                     SciEngines_API_Core/lane_phy_con[10].cni_lane_ibuf
                                                       ProtoComp153.IMUX.20
    ILOGIC_X16Y173.D     net (fanout=1)        0.124   SciEngines_API_Core/cniLane_rx<10>
    ILOGIC_X16Y173.CLK1  Tiockd      (-Th)    -0.501   SciEngines_API_Core/cniLane_fd0<21>
                                                       ProtoComp163.D2OFFBYP_SRC.20
                                                     SciEngines_API_Core/lane_phy_con[10].cni_DDR
    -------------------------------------------------  ---------------------------
```

```
2893    Total                                          0.946ns (0.822ns logic, 0.124ns route)
2894                                                           (86.9% logic, 13.1% route)
2895
2896  Maximum Clock Path at Fast Process Corner: CNI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[10].cni_DDR
2897    Location             Delay type         Delay(ns)  Physical Resource
2898                                                       Logical Resource(s)
2899    -------------------------------------------------  -------------------
2900    B14.I                Tiopi                 0.367   CNI_CLK
2901                                                       CNI_CLK
2902                                              SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
2903                                                       ProtoComp162.IMUX
2904    BUFIO2_X2Y26.I       net (fanout=1)        0.213
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkin1
2905    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2906                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2907    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2908    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
2909                                                    SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                           ↪  ll_base_inst/PLL_ADV
2910    BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkout1
2911    BUFGMUX_X2Y1.O       Tgi0o                 0.063
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2912                                            SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2913    ILOGIC_X16Y173.CLK1  net (fanout=241)      1.036   SciEngines_API_Core/cni_dom
2914    -------------------------------------------------  ---------------------------
2915    Total                                       -0.109ns (-1.909ns logic, 1.800ns route)
2916
2917 --------------------------------------------------------------------------------
2918 Slack (hold path):      7.534ns (requirement - (clock path + clock arrival + uncertainty -
    ↪  data path))
2919   Source:               CNI<10> (PAD)
2920   Destination:          SciEngines_API_Core/lane_phy_con[10].cni_DDR (FF)
2921   Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
2922   Requirement:          6.400ns
2923   Data Path Delay:      0.946ns (Levels of Logic = 2)
2924   Clock Path Delay:     -0.034ns (Levels of Logic = 4)
2925   Clock Uncertainty:    0.262ns
2926
2927   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
2928     Total System Jitter (TSJ):  0.050ns
2929     Discrete Jitter (DJ):       0.181ns
2930     Phase Error (PE):           0.167ns
2931
```

```
2932  Minimum Data Path at Fast Process Corner: CNI<10> to
      ↪  SciEngines_API_Core/lane_phy_con[10].cni_DDR
2933    Location             Delay type         Delay(ns)  Physical Resource
2934                                                       Logical Resource(s)
2935    ---------------------------------------------------  -------------------
2936    D12.I                Tiopi                 0.321   CNI<10>
2937                                                       CNI<10>
2938                                                     SciEngines_API_Core/lane_phy_con[10].┘
                                                           ↪  cni_lane_ibuf
2939                                                       ProtoComp153.IMUX.20
2940    ILOGIC_X16Y173.D     net (fanout=1)        0.124   SciEngines_API_Core/cniLane_rx<10>
2941    ILOGIC_X16Y173.CLK0  Tiockd      (-Th)    -0.501   SciEngines_API_Core/cniLane_fd0<21>
2942                                                       ProtoComp163.D2OFFBYP_SRC.20
2943                                                   SciEngines_API_Core/lane_phy_con[10].cni_DDR
2944    ---------------------------------------------------  ---------------------------
2945    Total                                      0.946ns (0.822ns logic, 0.124ns route)
2946                                                       (86.9% logic, 13.1% route)
2947
2948  Maximum Clock Path at Fast Process Corner: CNI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[10].cni_DDR
2949    Location             Delay type         Delay(ns)  Physical Resource
2950                                                       Logical Resource(s)
2951    ---------------------------------------------------  -------------------
2952    B14.I                Tiopi                 0.367   CNI_CLK
2953                                                       CNI_CLK
2954                                                 SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
2955                                                       ProtoComp162.IMUX
2956    BUFIO2_X2Y26.I       net (fanout=1)        0.213
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkin1
2957    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2958                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
2959    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
2960    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
2961                                                     SciEngines_API_Core/api_clk_mgmt_dn/p┘
                                                           ↪  ll_base_inst/PLL_ADV
2962    BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkout1
2963    BUFGMUX_X2Y1.O       Tgi0o                 0.063
        ↪  SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2964                                               SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
2965    ILOGIC_X16Y173.CLK0  net (fanout=241)      1.111   SciEngines_API_Core/cni_dom
2966    ---------------------------------------------------  ---------------------------
2967    Total                                     -0.034ns (-1.909ns logic, 1.875ns route)
2968
2969  --------------------------------------------------------------------------------
```

```
2970
2971 Paths for end point SciEngines_API_Core/lane_phy_con[16].cni_DDR (ILOGIC_X12Y173.D), 2
     ↪ paths
2972 --------------------------------------------------------------------------------
2973 Slack (hold path):      2.611ns (requirement - (clock path + clock arrival + uncertainty -
     ↪ data path))
2974   Source:               CNI<16> (PAD)
2975   Destination:          SciEngines_API_Core/lane_phy_con[16].cni_DDR (FF)
2976   Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
2977   Requirement:          6.400ns
2978   Data Path Delay:      0.946ns (Levels of Logic = 2)
2979   Clock Path Delay:     -0.111ns (Levels of Logic = 4)
2980   Clock Uncertainty:    0.262ns
2981
2982   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
2983     Total System Jitter (TSJ):  0.050ns
2984     Discrete Jitter (DJ):       0.181ns
2985     Phase Error (PE):           0.167ns
2986
2987   Minimum Data Path at Fast Process Corner: CNI<16> to
       ↪ SciEngines_API_Core/lane_phy_con[16].cni_DDR
2988     Location             Delay type         Delay(ns)  Physical Resource
2989                                                        Logical Resource(s)
2990     -------------------------------------------------  -------------------
2991     C11.I                Tiopi                 0.321   CNI<16>
2992                                                        CNI<16>
2993                                                      SciEngines_API_Core/lane_phy_con[16].
                                                           ↪ cni_lane_ibuf
2994                                                        ProtoComp153.IMUX.26
2995     ILOGIC_X12Y173.D     net (fanout=1)        0.124   SciEngines_API_Core/cniLane_rx<16>
2996     ILOGIC_X12Y173.CLK1  Tiockd      (-Th)    -0.501  SciEngines_API_Core/cniLane_fd0<33>
2997                                                        ProtoComp163.D2OFFBYP_SRC.26
2998                                                    SciEngines_API_Core/lane_phy_con[16].cni_DDR
2999     -------------------------------------------------  ---------------------------
3000     Total                                      0.946ns (0.822ns logic, 0.124ns route)
3001                                                        (86.9% logic, 13.1% route)
3002
3003   Maximum Clock Path at Fast Process Corner: CNI_CLK to
       ↪ SciEngines_API_Core/lane_phy_con[16].cni_DDR
3004     Location             Delay type         Delay(ns)  Physical Resource
3005                                                        Logical Resource(s)
3006     -------------------------------------------------  -------------------
3007     B14.I                Tiopi                 0.367   CNI_CLK
3008                                                        CNI_CLK
3009                                                  SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
3010                                                        ProtoComp162.IMUX
3011     BUFIO2_X2Y26.I       net (fanout=1)        0.213
       ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
```

```
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                     SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                       ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X12Y173.CLK1  net (fanout=241)      1.034   SciEngines_API_Core/cni_dom
    ---------------------------------------------------  ---------------------------
    Total                                     -0.111ns (-1.909ns logic, 1.798ns route)

--------------------------------------------------------------------------------
Slack (hold path):      7.536ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CNI<16> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[16].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
  Requirement:          6.400ns
  Data Path Delay:      0.946ns (Levels of Logic = 2)
  Clock Path Delay:     -0.036ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CNI<16> to
    ↪ SciEngines_API_Core/lane_phy_con[16].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    C11.I                Tiopi                 0.321   CNI<16>
                                                       CNI<16>
                                                     SciEngines_API_Core/lane_phy_con[16].⌋
                                                       ↪ cni_lane_ibuf
                                                       ProtoComp153.IMUX.26
    ILOGIC_X12Y173.D     net (fanout=1)        0.124   SciEngines_API_Core/cniLane_rx<16>
    ILOGIC_X12Y173.CLK0  Tiockd      (-Th)    -0.501   SciEngines_API_Core/cniLane_fd0<33>
                                                       ProtoComp163.D2OFFBYP_SRC.26
                                             SciEngines_API_Core/lane_phy_con[16].cni_DDR
```

```
    ------------------------------------------------  ---------------------------
    Total                                          0.946ns (0.822ns logic, 0.124ns route)
                                                           (86.9% logic, 13.1% route)

  Maximum Clock Path at Fast Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[16].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    B14.I                Tiopi                 0.367   CNI_CLK
                                                       CNI_CLK
                                            SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                       ProtoComp162.IMUX
    BUFIO2_X2Y26.I       net (fanout=1)        0.213
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                  SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                     ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.063
      ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X12Y173.CLK0  net (fanout=241)      1.109   SciEngines_API_Core/cni_dom
    ------------------------------------------------  ---------------------------
    Total                                       -0.036ns (-1.909ns logic, 1.873ns route)

--------------------------------------------------------------------------------

Paths for end point SciEngines_API_Core/lane_phy_con[11].cni_DDR (ILOGIC_X16Y174.D), 2
  ↪ paths
--------------------------------------------------------------------------------
Slack (hold path):      2.640ns (requirement - (clock path + clock arrival + uncertainty -
  ↪ data path))
  Source:               CNI<11> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[11].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom falling at 4.584ns
  Requirement:          6.400ns
  Data Path Delay:      0.978ns (Levels of Logic = 2)
  Clock Path Delay:     -0.108ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns
```

```
Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Minimum Data Path at Fast Process Corner: CNI<11> to
  ↪ SciEngines_API_Core/lane_phy_con[11].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  E12.I                Tiopi                 0.321   CNI<11>
                                                     CNI<11>
                                                   SciEngines_API_Core/lane_phy_con[11].
                                                     ↪ cni_lane_ibuf
                                                     ProtoComp153.IMUX.21
  ILOGIC_X16Y174.D     net (fanout=1)        0.156   SciEngines_API_Core/cniLane_rx<11>
  ILOGIC_X16Y174.CLK1  Tiockd      (-Th)    -0.501   SciEngines_API_Core/cniLane_fd0<23>
                                                     ProtoComp163.D2OFFBYP_SRC.21
                                                 SciEngines_API_Core/lane_phy_con[11].cni_DDR
  -------------------------------------------------  ---------------------------
  Total                                      0.978ns (0.822ns logic, 0.156ns route)
                                                     (84.0% logic, 16.0% route)

Maximum Clock Path at Fast Process Corner: CNI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[11].cni_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  B14.I                Tiopi                 0.367   CNI_CLK
                                                     CNI_CLK
                                              SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                     ProtoComp162.IMUX
  BUFIO2_X2Y26.I       net (fanout=1)        0.213
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
  BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
  PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                   SciEngines_API_Core/api_clk_mgmt_dn/p
                                                     ↪ ll_base_inst/PLL_ADV
  BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
  BUFGMUX_X2Y1.O       Tgi0o                 0.063
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                            SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
```

```
    ILOGIC_X16Y174.CLK1  net (fanout=241)      1.037   SciEngines_API_Core/cni_dom
    ---------------------------------------------------  ---------------------------
    Total                                      -0.108ns (-1.909ns logic, 1.801ns route)

--------------------------------------------------------------------------------
Slack (hold path):      7.566ns (requirement - (clock path + clock arrival + uncertainty -
    ↪ data path))
  Source:               CNI<11> (PAD)
  Destination:          SciEngines_API_Core/lane_phy_con[11].cni_DDR (FF)
  Destination Clock:    SciEngines_API_Core/cni_dom rising at -0.416ns
  Requirement:          6.400ns
  Data Path Delay:      0.978ns (Levels of Logic = 2)
  Clock Path Delay:     -0.034ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Data Path at Fast Process Corner: CNI<11> to
    ↪ SciEngines_API_Core/lane_phy_con[11].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    E12.I                Tiopi                 0.321   CNI<11>
                                                       CNI<11>
                                                     SciEngines_API_Core/lane_phy_con[11].┘
                                                       ↪ cni_lane_ibuf
                                                       ProtoComp153.IMUX.21
    ILOGIC_X16Y174.D     net (fanout=1)        0.156   SciEngines_API_Core/cniLane_rx<11>
    ILOGIC_X16Y174.CLK0  Tiockd      (-Th)    -0.501   SciEngines_API_Core/cniLane_fd0<23>
                                                       ProtoComp163.D2OFFBYP_SRC.21
                                                    SciEngines_API_Core/lane_phy_con[11].cni_DDR
    ---------------------------------------------------  ---------------------------
    Total                                       0.978ns (0.822ns logic, 0.156ns route)
                                                       (84.0% logic, 16.0% route)

  Maximum Clock Path at Fast Process Corner: CNI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[11].cni_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------------  -------------------
    B14.I                Tiopi                 0.367   CNI_CLK
                                                       CNI_CLK
                                                  SciEngines_API_Core/api_clk_mgmt_dn/clkin1_buf
                                                       ProtoComp162.IMUX
```

```
    BUFIO2_X2Y26.I       net (fanout=1)        0.213
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkin1
    BUFIO2_X2Y26.DIVCLK  Tbufcko_DIVCLK        0.130   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_0
    PLL_ADV_X0Y3.CLKIN1  net (fanout=1)        0.339
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y3.CLKOUT1 Tpllcko_CLK          -2.469
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/pll_base_inst/PLL_ADV
                                                     SciEngines_API_Core/api_clk_mgmt_dn/p⌋
                                                       ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y1.I0      net (fanout=1)        0.212
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout1
    BUFGMUX_X2Y1.O       Tgi0o                 0.063
    ↪ SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
                                           SciEngines_API_Core/api_clk_mgmt_dn/clkout2_buf
    ILOGIC_X16Y174.CLK0  net (fanout=241)      1.111   SciEngines_API_Core/cni_dom
    ---------------------------------------------  ---------------------------
    Total                                    -0.034ns (-1.909ns logic, 1.875ns route)

--------------------------------------------------------------------------------

================================================================================
Timing constraint: TIMEGRP "TNM_CNO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
For more information, see Offset Out Analysis in the Timing Closure User Guide (UG612).

 17 paths analyzed, 17 endpoints analyzed, 0 failing endpoints
 0 timing errors detected.
 Minimum allowable offset is   2.361ns.
--------------------------------------------------------------------------------

Paths for end point CNO<13> (D13.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  0.569ns (requirement - (clock arrival + clock path + data path +
  ↪ uncertainty))
  Source:               SciEngines_API_Core/lane_phy_con[13].cno_DDR (FF)
  Destination:          CNO<13> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          2.930ns
  Data Path Delay:      3.575ns (Levels of Logic = 1)
  Clock Path Delay:     -1.060ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns
```

```
3210  Maximum Clock Path at Slow Process Corner: CPI_CLK to
      ↪  SciEngines_API_Core/lane_phy_con[13].cno_DDR
3211    Location             Delay type         Delay(ns)  Physical Resource
3212                                                       Logical Resource(s)
3213    ---------------------------------------------------  -------------------
3214    AF12.I               Tiopi                 0.790   CPI_CLK
3215                                                       CPI_CLK
3216                                           SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
3217                                                       ProtoComp162.IMUX.1
3218    BUFIO2_X1Y7.I        net (fanout=1)        0.396
        ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
3219    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
3220                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
3221    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
        ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
3222    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
        ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
3223                                                 SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                        ↪  ll_base_inst/PLL_ADV
3224    BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
        ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout0
3225    BUFGMUX_X2Y4.O       Tgi0o                 0.209
        ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
3226                                           SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
3227    OLOGIC_X17Y172.CLK0  net (fanout=1608)     1.908   SciEngines_API_Core/clk_int
3228    ---------------------------------------------------  ---------------------------
3229    Total                                     -1.060ns (-4.352ns logic, 3.292ns route)
3230
3231  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[13].cno_DDR to
      ↪  CNO<13>
3232    Location             Delay type         Delay(ns)  Physical Resource
3233                                                       Logical Resource(s)
3234    ---------------------------------------------------  -------------------
3235    OLOGIC_X17Y172.OQ    Tockq                 0.742   SciEngines_API_Core/cnoLane_tx<13>
3236                                             SciEngines_API_Core/lane_phy_con[13].cno_DDR
3237    D13.O                net (fanout=1)        0.362   SciEngines_API_Core/cnoLane_tx<13>
3238    D13.PAD              Tioop                 2.471   CNO<13>
3239                                                 SciEngines_API_Core/lane_phy_con[13].⌋
                                                        ↪  cno_lane_obuf
3240                                                       CNO<13>
3241    ---------------------------------------------------  ---------------------------
3242    Total                                     3.575ns (3.213ns logic, 0.362ns route)
3243                                                       (89.9% logic, 10.1% route)
3244
3245 --------------------------------------------------------------------------------
3246
3247 Paths for end point CNO<4> (B12.PAD), 1 path
```

```
3248 ------------------------------------------------------------------------------
3249 Slack (slowest paths):  0.571ns (requirement - (clock arrival + clock path + data path +
     ↪  uncertainty))
3250   Source:               SciEngines_API_Core/lane_phy_con[4].cno_DDR (FF)
3251   Destination:          CNO<4> (PAD)
3252   Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
3253   Requirement:          2.930ns
3254   Data Path Delay:      3.575ns (Levels of Logic = 1)
3255   Clock Path Delay:     -1.062ns (Levels of Logic = 4)
3256   Clock Uncertainty:    0.262ns
3257
3258   Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
3259     Total System Jitter (TSJ):  0.050ns
3260     Discrete Jitter (DJ):       0.181ns
3261     Phase Error (PE):           0.167ns
3262
3263   Maximum Clock Path at Slow Process Corner: CPI_CLK to
       ↪  SciEngines_API_Core/lane_phy_con[4].cno_DDR
3264     Location             Delay type         Delay(ns)  Physical Resource
3265                                                        Logical Resource(s)
3266     -------------------------------------------------  -------------------
3267     AF12.I               Tiopi                 0.790   CPI_CLK
3268                                                        CPI_CLK
3269                                               SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
3270                                                        ProtoComp162.IMUX.1
3271     BUFIO2_X1Y7.I        net (fanout=1)        0.396
       ↪  SciEngines_API_Core/api_clk_mgmt_up/clkin1
3272     BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
3273                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
3274     PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
       ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
3275     PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
       ↪  SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
3276                                                   SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                         ↪  ll_base_inst/PLL_ADV
3277     BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
       ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout0
3278     BUFGMUX_X2Y4.O       Tgi0o                 0.209
       ↪  SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
3279                                              SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
3280     OLOGIC_X13Y173.CLK0  net (fanout=1608)     1.906   SciEngines_API_Core/clk_int
3281     -------------------------------------------------  ---------------------------
3282     Total                                     -1.062ns (-4.352ns logic, 3.290ns route)
3283
3284   Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[4].cno_DDR to
       ↪  CNO<4>
3285     Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    OLOGIC_X13Y173.OQ    Tockq                 0.742   SciEngines_API_Core/cnoLane_tx<4>
                                                        SciEngines_API_Core/lane_phy_con[4].cno_DDR
    B12.O                net (fanout=1)        0.362   SciEngines_API_Core/cnoLane_tx<4>
    B12.PAD              Tioop                 2.471   CNO<4>
                                                      SciEngines_API_Core/lane_phy_con[4].cno_lane_obuf
                                                        CNO<4>
    ---------------------------------------------------  ---------------------------
    Total                                      3.575ns (3.213ns logic, 0.362ns route)
                                                        (89.9% logic, 10.1% route)

--------------------------------------------------------------------------------

Paths for end point CNO<5> (A12.PAD), 1 path
--------------------------------------------------------------------------------
Slack (slowest paths):  0.571ns (requirement - (clock arrival + clock path + data path +
  ↪ uncertainty))
  Source:               SciEngines_API_Core/lane_phy_con[5].cno_DDR (FF)
  Destination:          CNO<5> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Requirement:          2.930ns
  Data Path Delay:      3.575ns (Levels of Logic = 1)
  Clock Path Delay:     -1.062ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Maximum Clock Path at Slow Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[5].cno_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    ---------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.790   CPI_CLK
                                                        CPI_CLK
                                                     SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                        ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.396
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.111   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                        SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.548
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -5.462
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
```

```
                                                    SciEngines_API_Core/api_clk_mgmt_up/p
                                                       ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.440
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.209
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    OLOGIC_X13Y172.CLK0  net (fanout=1608)     1.906   SciEngines_API_Core/clk_int
    ------------------------------------------------  ---------------------------
    Total                                    -1.062ns (-4.352ns logic, 3.290ns route)

  Maximum Data Path at Slow Process Corner: SciEngines_API_Core/lane_phy_con[5].cno_DDR to
    ↪ CNO<5>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    OLOGIC_X13Y172.OQ    Tockq                 0.742   SciEngines_API_Core/cnoLane_tx<5>
                                                        SciEngines_API_Core/lane_phy_con[5].cno_DDR
    A12.O                net (fanout=1)        0.362   SciEngines_API_Core/cnoLane_tx<5>
    A12.PAD              Tioop                 2.471   CNO<5>
                                         SciEngines_API_Core/lane_phy_con[5].cno_lane_obuf
                                                       CNO<5>
    ------------------------------------------------  ---------------------------
    Total                                    3.575ns (3.213ns logic, 0.362ns route)
                                                       (89.9% logic, 10.1% route)

--------------------------------------------------------------------------------

Fastest Paths: TIMEGRP "TNM_CNO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
--------------------------------------------------------------------------------

Paths for end point CNO<3> (J13.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  1.084ns (clock arrival + clock path + data path - uncertainty)
  Source:               SciEngines_API_Core/lane_phy_con[3].cno_DDR (FF)
  Destination:          CNO<3> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Data Path Delay:      2.168ns (Levels of Logic = 1)
  Clock Path Delay:     -0.406ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Clock Path at Fast Process Corner: CPI_CLK to
    ↪ SciEngines_API_Core/lane_phy_con[3].cno_DDR
```

```
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    AF12.I               Tiopi                 0.321   CPI_CLK
                                                       CPI_CLK
                                            SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.203
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
      ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                  SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                    ↪ ll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
    BUFGMUX_X2Y4.O       Tgi0o                 0.059
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    OLOGIC_X24Y175.CLK0  net (fanout=1608)     0.743   SciEngines_API_Core/clk_int
    -------------------------------------------------  ---------------------------
    Total                                   -0.406ns (-1.786ns logic, 1.380ns route)

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[3].cno_DDR to
    ↪ CNO<3>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    OLOGIC_X24Y175.OQ    Tockq                 0.419   SciEngines_API_Core/cnoLane_tx<3>
                                             SciEngines_API_Core/lane_phy_con[3].cno_DDR
    J13.O                net (fanout=1)        0.268   SciEngines_API_Core/cnoLane_tx<3>
    J13.PAD              Tioop                 1.481   CNO<3>
                                          SciEngines_API_Core/lane_phy_con[3].cno_lane_obuf
                                                       CNO<3>
    -------------------------------------------------  ---------------------------
    Total                                    2.168ns (1.900ns logic, 0.268ns route)
                                                       (87.6% logic, 12.4% route)

--------------------------------------------------------------------------------

Paths for end point CNO<14> (D14.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  1.085ns (clock arrival + clock path + data path - uncertainty)
  Source:               SciEngines_API_Core/lane_phy_con[14].cno_DDR (FF)
```

```
Destination:          CNO<14> (PAD)
Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
Data Path Delay:      2.168ns (Levels of Logic = 1)
Clock Path Delay:     -0.405ns (Levels of Logic = 4)
Clock Uncertainty:    0.262ns

Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
  Total System Jitter (TSJ):  0.050ns
  Discrete Jitter (DJ):       0.181ns
  Phase Error (PE):           0.167ns

Minimum Clock Path at Fast Process Corner: CPI_CLK to
  ↪ SciEngines_API_Core/lane_phy_con[14].cno_DDR
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  AF12.I               Tiopi                 0.321   CPI_CLK
                                                     CPI_CLK
                                          SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                     ProtoComp162.IMUX.1
  BUFIO2_X1Y7.I        net (fanout=1)        0.203
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkin1
  BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                     SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
  PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
  ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
  PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
  ↪ SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                   SciEngines_API_Core/api_clk_mgmt_up/p⌋
                                                     ↪ ll_base_inst/PLL_ADV
  BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout0
  BUFGMUX_X2Y4.O       Tgi0o                 0.059
  ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                        SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
  OLOGIC_X19Y175.CLK0  net (fanout=1608)     0.744   SciEngines_API_Core/clk_int
  -------------------------------------------------  ---------------------------
  Total                                     -0.405ns (-1.786ns logic, 1.381ns route)

Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[14].cno_DDR to
  ↪ CNO<14>
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  OLOGIC_X19Y175.OQ    Tockq                 0.419   SciEngines_API_Core/cnoLane_tx<14>
                                                   SciEngines_API_Core/lane_phy_con[14].cno_DDR
  D14.O                net (fanout=1)        0.268   SciEngines_API_Core/cnoLane_tx<14>
```

```
    D14.PAD              Tioop                 1.481   CNO<14>
                                                       SciEngines_API_Core/lane_phy_con[14].cno_lane_obuf
                                                       CNO<14>
    ---------------------------------------------  ---------------------------
    Total                                      2.168ns (1.900ns logic, 0.268ns route)
                                                       (87.6% logic, 12.4% route)

--------------------------------------------------------------------------------

Paths for end point CNO<15> (G14.PAD), 1 path
--------------------------------------------------------------------------------
Delay (fastest paths):  1.086ns (clock arrival + clock path + data path - uncertainty)
  Source:               SciEngines_API_Core/lane_phy_con[15].cno_DDR (FF)
  Destination:          CNO<15> (PAD)
  Source Clock:         SciEngines_API_Core/clk_int rising at -0.416ns
  Data Path Delay:      2.168ns (Levels of Logic = 1)
  Clock Path Delay:     -0.404ns (Levels of Logic = 4)
  Clock Uncertainty:    0.262ns

  Clock Uncertainty:          0.262ns  ((TSJ^2 + DJ^2)^1/2) / 2 + PE
    Total System Jitter (TSJ):  0.050ns
    Discrete Jitter (DJ):       0.181ns
    Phase Error (PE):           0.167ns

  Minimum Clock Path at Fast Process Corner: CPI_CLK to
    SciEngines_API_Core/lane_phy_con[15].cno_DDR
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ---------------------------------------------  -------------------
    AF12.I               Tiopi                 0.321   CPI_CLK
                                                       CPI_CLK
                                           SciEngines_API_Core/api_clk_mgmt_up/clkin1_buf
                                                       ProtoComp162.IMUX.1
    BUFIO2_X1Y7.I        net (fanout=1)        0.203
      SciEngines_API_Core/api_clk_mgmt_up/clkin1
    BUFIO2_X1Y7.DIVCLK   Tbufcko_DIVCLK        0.122   SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
                                                       SP6_BUFIO2_INSERT_PLL1_ML_BUFIO2_1
    PLL_ADV_X0Y2.CLKIN2  net (fanout=1)        0.306
      SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV_ML_NEW_DIVCLK
    PLL_ADV_X0Y2.CLKOUT0 Tpllcko_CLK          -2.288
      SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
                                                       SciEngines_API_Core/api_clk_mgmt_up/pll_base_inst/PLL_ADV
    BUFGMUX_X2Y4.I0      net (fanout=1)        0.128
      SciEngines_API_Core/api_clk_mgmt_up/clkout0
```

```
    BUFGMUX_X2Y4.O       Tgi0o                 0.059
      ↪ SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
                                          SciEngines_API_Core/api_clk_mgmt_up/clkout1_buf
    OLOGIC_X23Y174.CLK0  net (fanout=1608)     0.745   SciEngines_API_Core/clk_int
    ------------------------------------------------  --------------------------
    Total                                    -0.404ns (-1.786ns logic, 1.382ns route)

  Minimum Data Path at Fast Process Corner: SciEngines_API_Core/lane_phy_con[15].cno_DDR to
    ↪ CNO<15>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    ------------------------------------------------  -------------------
    OLOGIC_X23Y174.OQ    Tockq                 0.419   SciEngines_API_Core/cnoLane_tx<15>
                                              SciEngines_API_Core/lane_phy_con[15].cno_DDR
    G14.O                net (fanout=1)        0.268   SciEngines_API_Core/cnoLane_tx<15>
    G14.PAD              Tioop                 1.481   CNO<15>
                                                   SciEngines_API_Core/lane_phy_con[15].
                                                     ↪ cno_lane_obuf
                                                   CNO<15>
    ------------------------------------------------  --------------------------
    Total                                     2.168ns (1.900ns logic, 0.268ns route)
                                                       (87.6% logic, 12.4% route)

--------------------------------------------------------------------------------


Derived Constraint Report
Derived Constraints for TS_CPI_CLK
+-------------------------------+-------------+-------------+-------------+-------------+
  ↪ -------------+-------------+-------------+
|                               |   Period    |      Actual Period      |     Timing Errors
  ↪ |      Paths Analyzed       |
|           Constraint          | Requirement
  ↪ |-------------+-------------|-------------+-------------|-------------+-------------|
|                               |             |   Direct    | Derivative  |   Direct    |
  ↪ Derivative  |   Direct    | Derivative  |
+-------------------------------+-------------+-------------+-------------+-------------+
  ↪ -------------+-------------+-------------+
|TS_CPI_CLK                     |     10.000ns|      3.334ns|     15.943ns|            0|
  ↪ 159|            0|     87301887|
| TS_SciEngines_API_Core_api_clk|     10.000ns|     15.943ns|          N/A|          159|
  ↪ 0|     87137019|            0|
| _mgmt_up_clkout1              |             |             |             |             |
  ↪ |             |             |
| TS_SciEngines_API_Core_api_clk|     10.000ns|      9.214ns|          N/A|            0|
  ↪ 0|       164868|            0|
```

```
| _mgmt_up_clkout0              |             |             |             |             |
↪  |             |             |
+-------------------------------+-------------+-------------+-------------+-------------+
↪  -------------+-------------+-------------+

Derived Constraints for TS_CNI_CLK
+-------------------------------+-------------+-------------+-------------+-------------+
↪  -------------+-------------+-------------+
|                               |   Period    |      Actual Period      |     Timing Errors
↪  |      Paths Analyzed       |
|           Constraint          | Requirement
↪  |-------------+-------------|-------------+-------------|-------------+-------------|
|                               |             |   Direct    | Derivative  |   Direct    |
↪  Derivative  |   Direct    | Derivative  |
+-------------------------------+-------------+-------------+-------------+-------------+
↪  -------------+-------------+-------------+
|TS_CNI_CLK                     |     10.000ns|      3.334ns|      7.954ns|            0|
↪  0|            0|         3001|
| TS_SciEngines_API_Core_api_clk|     10.000ns|      7.954ns|          N/A|            0|
↪  0|         3001|            0|
| _mgmt_dn_clkout1              |             |             |             |             |
↪  |             |             |
+-------------------------------+-------------+-------------+-------------+-------------+
↪  -------------+-------------+-------------+


1 constraint not met.


Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock CNI_CLK
------------+------------+------------+------------+------------+-----------------------+
↪  ---+--------+
            |Max Setup to|  Process   |Max Hold to |  Process   |                       |
             ↪  Clock  |
Source      | clk (edge) |   Corner   | clk (edge) |   Corner   |Internal Clock(s)
↪  | Phase  |
------------+------------+------------+------------+------------+-----------------------+
↪  ---+--------+
CNI<0>      |    2.598(R)|      SLOW  |   -1.321(R)|      FAST
↪  |SciEngines_API_Core/cni_dom|  -0.416|
            |   -2.396(F)|      SLOW  |    3.604(F)|      FAST
             ↪  |SciEngines_API_Core/cni_dom|   4.584|
CNI<1>      |    2.550(R)|      SLOW  |   -1.292(R)|      FAST
↪  |SciEngines_API_Core/cni_dom|  -0.416|
```

```
3553             |   -2.444(F)|      SLOW  |    3.633(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3554 CNI<2>      |    2.611(R)|      SLOW  |   -1.353(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3555             |   -2.384(F)|      SLOW  |    3.573(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3556 CNI<3>      |    2.607(R)|      SLOW  |   -1.349(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3557             |   -2.387(F)|      SLOW  |    3.576(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3558 CNI<4>      |    2.595(R)|      SLOW  |   -1.318(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3559             |   -2.400(F)|      SLOW  |    3.608(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3560 CNI<5>      |    2.547(R)|      SLOW  |   -1.289(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3561             |   -2.448(F)|      SLOW  |    3.637(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3562 CNI<6>      |    2.655(R)|      SLOW  |   -1.378(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3563             |   -2.339(F)|      SLOW  |    3.547(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3564 CNI<7>      |    2.596(R)|      SLOW  |   -1.319(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3565             |   -2.398(F)|      SLOW  |    3.606(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3566 CNI<8>      |    2.608(R)|      SLOW  |   -1.350(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3567             |   -2.386(F)|      SLOW  |    3.575(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3568 CNI<9>      |    2.426(R)|      SLOW  |   -1.168(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3569             |   -2.569(F)|      SLOW  |    3.758(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3570 CNI<10>     |    2.411(R)|      SLOW  |   -1.134(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3571             |   -2.583(F)|      SLOW  |    3.791(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3572 CNI<11>     |    2.424(R)|      SLOW  |   -1.166(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3573             |   -2.571(F)|      SLOW  |    3.760(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
3574 CNI<12>     |    2.595(R)|      SLOW  |   -1.318(R)|      FAST
     ↪  |SciEngines_API_Core/cni_dom|  -0.416|
3575             |   -2.399(F)|      SLOW  |    3.607(F)|      FAST
                 ↪  |SciEngines_API_Core/cni_dom|   4.584|
```

```
CNI<13>     |    2.547(R)|      SLOW  |   -1.289(R)|      FAST    |SciEngines_API_Core/cni_dom|  -0.416|
            |   -2.447(F)|      SLOW  |    3.636(F)|      FAST    |SciEngines_API_Core/cni_dom|   4.584|
CNI<14>     |    2.656(R)|      SLOW  |   -1.379(R)|      FAST    |SciEngines_API_Core/cni_dom|  -0.416|
            |   -2.338(F)|      SLOW  |    3.546(F)|      FAST    |SciEngines_API_Core/cni_dom|   4.584|
CNI<15>     |    2.472(R)|      SLOW  |   -1.195(R)|      FAST    |SciEngines_API_Core/cni_dom|  -0.416|
            |   -2.523(F)|      SLOW  |    3.731(F)|      FAST    |SciEngines_API_Core/cni_dom|   4.584|
CNI<16>     |    2.413(R)|      SLOW  |   -1.136(R)|      FAST    |SciEngines_API_Core/cni_dom|  -0.416|
            |   -2.581(F)|      SLOW  |    3.789(F)|      FAST    |SciEngines_API_Core/cni_dom|   4.584|
------------+------------+------------+------------+------------+-----------------------+--------+

Setup/Hold to clock CPI_CLK
------------+------------+------------+------------+------------+-----------------------+--------+
            |Max Setup to|  Process   |Max Hold to |  Process   |                       |        |
            |  Clock  |
Source      | clk (edge) |   Corner   | clk (edge) |   Corner   |Internal Clock(s)      | Phase  |
------------+------------+------------+------------+------------+-----------------------+--------+
CPI<0>      |    2.366(R)|      SLOW  |   -1.177(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
            |   -2.628(F)|      SLOW  |    3.748(F)|      FAST    |SciEngines_API_Core/clk_int|   4.584|
CPI<1>      |    2.414(R)|      SLOW  |   -1.206(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
            |   -2.580(F)|      SLOW  |    3.719(F)|      FAST    |SciEngines_API_Core/clk_int|   4.584|
CPI<2>      |    2.599(R)|      SLOW  |   -1.391(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
            |   -2.395(F)|      SLOW  |    3.534(F)|      FAST    |SciEngines_API_Core/clk_int|   4.584|
CPI<3>      |    2.426(R)|      SLOW  |   -1.237(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
            |   -2.568(F)|      SLOW  |    3.688(F)|      FAST    |SciEngines_API_Core/clk_int|   4.584|
CPI<4>      |    2.418(R)|      SLOW  |   -1.210(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
```

```
3600             |   -2.577(F)|      SLOW  |    3.716(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3601 CPI<5>      |    2.370(R)|      SLOW  |   -1.181(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3602             |   -2.625(F)|      SLOW  |    3.745(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3603 CPI<6>      |    2.426(R)|      SLOW  |   -1.237(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3604             |   -2.568(F)|      SLOW  |    3.688(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3605 CPI<7>      |    2.660(R)|      SLOW  |   -1.452(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3606             |   -2.335(F)|      SLOW  |    3.474(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3607 CPI<8>      |    2.612(R)|      SLOW  |   -1.423(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3608             |   -2.383(F)|      SLOW  |    3.503(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3609 CPI<9>      |    2.550(R)|      SLOW  |   -1.361(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3610             |   -2.444(F)|      SLOW  |    3.564(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3611 CPI<10>     |    2.478(R)|      SLOW  |   -1.270(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3612             |   -2.517(F)|      SLOW  |    3.656(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3613 CPI<11>     |    2.474(R)|      SLOW  |   -1.266(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3614             |   -2.520(F)|      SLOW  |    3.659(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3615 CPI<12>     |    2.618(R)|      SLOW  |   -1.429(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3616             |   -2.376(F)|      SLOW  |    3.496(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3617 CPI<13>     |    2.661(R)|      SLOW  |   -1.453(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3618             |   -2.333(F)|      SLOW  |    3.472(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3619 CPI<14>     |    2.666(R)|      SLOW  |   -1.458(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3620             |   -2.329(F)|      SLOW  |    3.468(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
3621 CPI<15>     |    2.553(R)|      SLOW  |   -1.364(R)|      FAST
     ↪  |SciEngines_API_Core/clk_int|  -0.416|
3622             |   -2.441(F)|      SLOW  |    3.561(F)|      FAST
                 ↪  |SciEngines_API_Core/clk_int|   4.584|
```

```
CPI<16>     |    2.419(R)|      SLOW  |   -1.211(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
            |   -2.576(F)|      SLOW  |    3.715(F)|      FAST    |SciEngines_API_Core/clk_int|   4.584|
------------+------------+------------+------------+------------+-----------------------+---+--------+

Clock CPI_CLK to Pad
------------+-----------------+------------+-----------------+------------+-------------+-------------+--------+
            |Max (slowest) clk|  Process   |Min (fastest) clk|  Process   |             |  Clock  |
Destination |  (edge) to PAD  |   Corner   |  (edge) to PAD  |   Corner   |Internal Clock(s)| Phase  |
------------+-----------------+------------+-----------------+------------+-------------+-------------+--------+
CNO<0>      |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<1>      |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<2>      |         2.124(R)|      SLOW  |         1.087(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<3>      |         2.121(R)|      SLOW  |         1.084(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<4>      |         2.359(R)|      SLOW  |         1.322(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<5>      |         2.359(R)|      SLOW  |         1.322(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<6>      |         2.173(R)|      SLOW  |         1.136(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<7>      |         2.125(R)|      SLOW  |         1.088(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<8>      |         2.125(R)|      SLOW  |         1.088(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<9>      |         2.124(R)|      SLOW  |         1.087(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<10>     |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<11>     |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<12>     |         2.308(R)|      SLOW  |         1.271(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<13>     |         2.361(R)|      SLOW  |         1.324(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<14>     |         2.122(R)|      SLOW  |         1.085(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
```

```
CNO<15>     |         2.123(R)|      SLOW  |         1.086(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CNO<16>     |         2.123(R)|      SLOW  |         1.086(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<0>      |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<1>      |         2.180(R)|      SLOW  |         1.143(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<2>      |         2.361(R)|      SLOW  |         1.324(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<3>      |         2.172(R)|      SLOW  |         1.135(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<4>      |         2.180(R)|      SLOW  |         1.143(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<5>      |         2.178(R)|      SLOW  |         1.141(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<6>      |         2.363(R)|      SLOW  |         1.326(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<7>      |         2.180(R)|      SLOW  |         1.143(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<8>      |         2.310(R)|      SLOW  |         1.273(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<9>      |         2.312(R)|      SLOW  |         1.275(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<10>     |         2.362(R)|      SLOW  |         1.325(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<11>     |         2.312(R)|      SLOW  |         1.275(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<12>     |         2.179(R)|      SLOW  |         1.142(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<13>     |         2.130(R)|      SLOW  |         1.093(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<14>     |         2.364(R)|      SLOW  |         1.327(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<15>     |         2.361(R)|      SLOW  |         1.324(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
CPO<16>     |         2.359(R)|      SLOW  |         1.322(R)|      FAST    |SciEngines_API_Core/clk_int|  -0.416|
------------+-----------------+------------+-----------------+------------+--------------+-------------+--------

Clock to Setup on destination clock CNI_CLK
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
CNI_CLK        |    7.954|         |         |         |
```

```
3674 ---------------+---------+---------+---------+---------+
3675
3676 Clock to Setup on destination clock CPI_CLK
3677 ---------------+---------+---------+---------+---------+
3678                | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
3679 Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
3680 ---------------+---------+---------+---------+---------+
3681 CPI_CLK        |   15.943|         |         |         |
3682 ---------------+---------+---------+---------+---------+
3683
3684 TIMEGRP "TNM_CPI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP "CPI_CLK";
3685 Worst Case Data Window 6.414; Ideal Clock Offset To Actual Clock 1.159;
3686 ------------------+------------+------------+------------+------------+---------+--------┐
     ↪  -+-------------+
3687                   |            |  Process   |            |  Process   |  Setup  |  Hold
                       ↪  |Source Offset|
3688 Source            |   Setup    |   Corner   |    Hold    |   Corner   |  Slack  |  Slack  |
     ↪  To Center  |
3689 ------------------+------------+------------+------------+------------+---------+--------┘
     ↪  -+-------------+
3690 CPI<0>            |    2.366(R)|      SLOW  |   -1.177(R)|      FAST  |    0.634|    7.577|
     ↪  -3.472|
3691                   |   -2.628(F)|      SLOW  |    3.748(F)|      FAST  |    5.628|    2.652|
                       ↪  1.488|
3692 CPI<1>            |    2.414(R)|      SLOW  |   -1.206(R)|      FAST  |    0.586|    7.606|
     ↪  -3.510|
3693                   |   -2.580(F)|      SLOW  |    3.719(F)|      FAST  |    5.580|    2.681|
                       ↪  1.450|
3694 CPI<2>            |    2.599(R)|      SLOW  |   -1.391(R)|      FAST  |    0.401|    7.791|
     ↪  -3.695|
3695                   |   -2.395(F)|      SLOW  |    3.534(F)|      FAST  |    5.395|    2.866|
                       ↪  1.264|
3696 CPI<3>            |    2.426(R)|      SLOW  |   -1.237(R)|      FAST  |    0.574|    7.637|
     ↪  -3.532|
3697                   |   -2.568(F)|      SLOW  |    3.688(F)|      FAST  |    5.568|    2.712|
                       ↪  1.428|
3698 CPI<4>            |    2.418(R)|      SLOW  |   -1.210(R)|      FAST  |    0.582|    7.610|
     ↪  -3.514|
3699                   |   -2.577(F)|      SLOW  |    3.716(F)|      FAST  |    5.577|    2.684|
                       ↪  1.446|
3700 CPI<5>            |    2.370(R)|      SLOW  |   -1.181(R)|      FAST  |    0.630|    7.581|
     ↪  -3.476|
3701                   |   -2.625(F)|      SLOW  |    3.745(F)|      FAST  |    5.625|    2.655|
                       ↪  1.485|
3702 CPI<6>            |    2.426(R)|      SLOW  |   -1.237(R)|      FAST  |    0.574|    7.637|
     ↪  -3.532|
```

```
3703                  |   -2.568(F)|      SLOW  |    3.688(F)|      FAST  |    5.568|    2.712|
                      ↪  1.428|
3704 CPI<7>           |    2.660(R)|      SLOW  |   -1.452(R)|      FAST  |    0.340|    7.852|
     ↪  -3.756|
3705                  |   -2.335(F)|      SLOW  |    3.474(F)|      FAST  |    5.335|    2.926|
                      ↪  1.204|
3706 CPI<8>           |    2.612(R)|      SLOW  |   -1.423(R)|      FAST  |    0.388|    7.823|
     ↪  -3.718|
3707                  |   -2.383(F)|      SLOW  |    3.503(F)|      FAST  |    5.383|    2.897|
                      ↪  1.243|
3708 CPI<9>           |    2.550(R)|      SLOW  |   -1.361(R)|      FAST  |    0.450|    7.761|
     ↪  -3.656|
3709                  |   -2.444(F)|      SLOW  |    3.564(F)|      FAST  |    5.444|    2.836|
                      ↪  1.304|
3710 CPI<10>          |    2.478(R)|      SLOW  |   -1.270(R)|      FAST  |    0.522|    7.670|
     ↪  -3.574|
3711                  |   -2.517(F)|      SLOW  |    3.656(F)|      FAST  |    5.517|    2.744|
                      ↪  1.387|
3712 CPI<11>          |    2.474(R)|      SLOW  |   -1.266(R)|      FAST  |    0.526|    7.666|
     ↪  -3.570|
3713                  |   -2.520(F)|      SLOW  |    3.659(F)|      FAST  |    5.520|    2.741|
                      ↪  1.389|
3714 CPI<12>          |    2.618(R)|      SLOW  |   -1.429(R)|      FAST  |    0.382|    7.829|
     ↪  -3.724|
3715                  |   -2.376(F)|      SLOW  |    3.496(F)|      FAST  |    5.376|    2.904|
                      ↪  1.236|
3716 CPI<13>          |    2.661(R)|      SLOW  |   -1.453(R)|      FAST  |    0.339|    7.853|
     ↪  -3.757|
3717                  |   -2.333(F)|      SLOW  |    3.472(F)|      FAST  |    5.333|    2.928|
                      ↪  1.203|
3718 CPI<14>          |    2.666(R)|      SLOW  |   -1.458(R)|      FAST  |    0.334|    7.858|
     ↪  -3.762|
3719                  |   -2.329(F)|      SLOW  |    3.468(F)|      FAST  |    5.329|    2.932|
                      ↪  1.198|
3720 CPI<15>          |    2.553(R)|      SLOW  |   -1.364(R)|      FAST  |    0.447|    7.764|
     ↪  -3.659|
3721                  |   -2.441(F)|      SLOW  |    3.561(F)|      FAST  |    5.441|    2.839|
                      ↪  1.301|
3722 CPI<16>          |    2.419(R)|      SLOW  |   -1.211(R)|      FAST  |    0.581|    7.611|
     ↪  -3.515|
3723                  |   -2.576(F)|      SLOW  |    3.715(F)|      FAST  |    5.576|    2.685|
                      ↪  1.445|
3724 ------------------+------------+------------+------------+------------+---------+--------⌋
     ↪  -+-------------+
3725 Worst Case Summary|       2.666|         -  |       3.748|         -  |    0.334|    2.652|
     ↪  |
```

```
------------------+------------+------------+------------+------------+---------+--------+
  -+-------------+

TIMEGRP "TNM_CNI" OFFSET = IN 3 ns VALID 9.4 ns BEFORE COMP "CNI_CLK";
Worst Case Data Window 6.447; Ideal Clock Offset To Actual Clock 1.133;
------------------+------------+------------+------------+------------+---------+--------+
  -+-------------+
                  |            | Process    |            | Process    | Setup   | Hold
                  |Source Offset|
Source            |   Setup    |   Corner   |    Hold    |   Corner   | Slack   | Slack  |
  To Center  |
------------------+------------+------------+------------+------------+---------+--------+
  -+-------------+
CNI<0>            |    2.598(R)|      SLOW  |   -1.321(R)|      FAST  |    0.402|    7.721|
  -3.660|
                  |   -2.396(F)|      SLOW  |    3.604(F)|      FAST  |    5.396|    2.796|
  1.300|
CNI<1>            |    2.550(R)|      SLOW  |   -1.292(R)|      FAST  |    0.450|    7.692|
  -3.621|
                  |   -2.444(F)|      SLOW  |    3.633(F)|      FAST  |    5.444|    2.767|
  1.339|
CNI<2>            |    2.611(R)|      SLOW  |   -1.353(R)|      FAST  |    0.389|    7.753|
  -3.682|
                  |   -2.384(F)|      SLOW  |    3.573(F)|      FAST  |    5.384|    2.827|
  1.279|
CNI<3>            |    2.607(R)|      SLOW  |   -1.349(R)|      FAST  |    0.393|    7.749|
  -3.678|
                  |   -2.387(F)|      SLOW  |    3.576(F)|      FAST  |    5.387|    2.824|
  1.281|
CNI<4>            |    2.595(R)|      SLOW  |   -1.318(R)|      FAST  |    0.405|    7.718|
  -3.657|
                  |   -2.400(F)|      SLOW  |    3.608(F)|      FAST  |    5.400|    2.792|
  1.304|
CNI<5>            |    2.547(R)|      SLOW  |   -1.289(R)|      FAST  |    0.453|    7.689|
  -3.618|
                  |   -2.448(F)|      SLOW  |    3.637(F)|      FAST  |    5.448|    2.763|
  1.343|
CNI<6>            |    2.655(R)|      SLOW  |   -1.378(R)|      FAST  |    0.345|    7.778|
  -3.717|
                  |   -2.339(F)|      SLOW  |    3.547(F)|      FAST  |    5.339|    2.853|
  1.243|
CNI<7>            |    2.596(R)|      SLOW  |   -1.319(R)|      FAST  |    0.404|    7.719|
  -3.658|
                  |   -2.398(F)|      SLOW  |    3.606(F)|      FAST  |    5.398|    2.794|
  1.302|
CNI<8>            |    2.608(R)|      SLOW  |   -1.350(R)|      FAST  |    0.392|    7.750|
  -3.679|
```

```
3751                  |   -2.386(F)|      SLOW  |    3.575(F)|      FAST  |    5.386|    2.825|
                      ↪  1.281|
3752 CNI<9>           |    2.426(R)|      SLOW  |   -1.168(R)|      FAST  |    0.574|    7.568|
     ↪  -3.497|
3753                  |   -2.569(F)|      SLOW  |    3.758(F)|      FAST  |    5.569|    2.642|
                      ↪  1.464|
3754 CNI<10>          |    2.411(R)|      SLOW  |   -1.134(R)|      FAST  |    0.589|    7.534|
     ↪  -3.473|
3755                  |   -2.583(F)|      SLOW  |    3.791(F)|      FAST  |    5.583|    2.609|
                      ↪  1.487|
3756 CNI<11>          |    2.424(R)|      SLOW  |   -1.166(R)|      FAST  |    0.576|    7.566|
     ↪  -3.495|
3757                  |   -2.571(F)|      SLOW  |    3.760(F)|      FAST  |    5.571|    2.640|
                      ↪  1.465|
3758 CNI<12>          |    2.595(R)|      SLOW  |   -1.318(R)|      FAST  |    0.405|    7.718|
     ↪  -3.657|
3759                  |   -2.399(F)|      SLOW  |    3.607(F)|      FAST  |    5.399|    2.793|
                      ↪  1.303|
3760 CNI<13>          |    2.547(R)|      SLOW  |   -1.289(R)|      FAST  |    0.453|    7.689|
     ↪  -3.618|
3761                  |   -2.447(F)|      SLOW  |    3.636(F)|      FAST  |    5.447|    2.764|
                      ↪  1.342|
3762 CNI<14>          |    2.656(R)|      SLOW  |   -1.379(R)|      FAST  |    0.344|    7.779|
     ↪  -3.718|
3763                  |   -2.338(F)|      SLOW  |    3.546(F)|      FAST  |    5.338|    2.854|
                      ↪  1.242|
3764 CNI<15>          |    2.472(R)|      SLOW  |   -1.195(R)|      FAST  |    0.528|    7.595|
     ↪  -3.534|
3765                  |   -2.523(F)|      SLOW  |    3.731(F)|      FAST  |    5.523|    2.669|
                      ↪  1.427|
3766 CNI<16>          |    2.413(R)|      SLOW  |   -1.136(R)|      FAST  |    0.587|    7.536|
     ↪  -3.475|
3767                  |   -2.581(F)|      SLOW  |    3.789(F)|      FAST  |    5.581|    2.611|
                      ↪  1.485|
3768 ------------------+------------+------------+------------+------------+---------+--------┘
     ↪  -+-------------+
3769 Worst Case Summary|       2.656|         -  |       3.791|         -  |    0.344|    2.609|
     ↪  |
3770 ------------------+------------+------------+------------+------------+---------+--------┘
     ↪  -+-------------+
3771
3772 TIMEGRP "TNM_CPO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
3773 Bus Skew: 0.234 ns;
3774 ------------------------------------------------+-------------+------------+-------------+┘
     ↪  ------------+--------------+
3775                                                  |Max (slowest)|  Process   |Min (fastest)|
                                                     ↪  Process   |            |
```

```
PAD                                             | Delay (ns)  |   Corner   | Delay (ns)  |   Corner   |Edge Skew (ns)|
-----------------------------------------------+------------+-----------+------------+-----------+--------------+
CPO<0>                                          |        2.310|      SLOW  |        1.273|      FAST  |         0.180|
CPO<1>                                          |        2.180|      SLOW  |        1.143|      FAST  |         0.050|
CPO<2>                                          |        2.361|      SLOW  |        1.324|      FAST  |         0.231|
CPO<3>                                          |        2.172|      SLOW  |        1.135|      FAST  |         0.042|
CPO<4>                                          |        2.180|      SLOW  |        1.143|      FAST  |         0.050|
CPO<5>                                          |        2.178|      SLOW  |        1.141|      FAST  |         0.048|
CPO<6>                                          |        2.363|      SLOW  |        1.326|      FAST  |         0.233|
CPO<7>                                          |        2.180|      SLOW  |        1.143|      FAST  |         0.050|
CPO<8>                                          |        2.310|      SLOW  |        1.273|      FAST  |         0.180|
CPO<9>                                          |        2.312|      SLOW  |        1.275|      FAST  |         0.182|
CPO<10>                                         |        2.362|      SLOW  |        1.325|      FAST  |         0.232|
CPO<11>                                         |        2.312|      SLOW  |        1.275|      FAST  |         0.182|
CPO<12>                                         |        2.179|      SLOW  |        1.142|      FAST  |         0.049|
CPO<13>                                         |        2.130|      SLOW  |        1.093|      FAST  |         0.000|
CPO<14>                                         |        2.364|      SLOW  |        1.327|      FAST  |         0.234|
CPO<15>                                         |        2.361|      SLOW  |        1.324|      FAST  |         0.231|
CPO<16>                                         |        2.359|      SLOW  |        1.322|      FAST  |         0.229|
-----------------------------------------------+------------+-----------+------------+-----------+--------------+

TIMEGRP "TNM_CNO" OFFSET = OUT 2.93 ns AFTER COMP "CPI_CLK";
Bus Skew: 0.240 ns;
-----------------------------------------------+------------+-----------+------------+-----------+--------------+
                                                |Max (slowest)|  Process   |Min (fastest)|  Process   |              |
```

```
PAD                                          | Delay (ns)  |   Corner   | Delay (ns)  |  Corner   |Edge Skew (ns)|
---------------------------------------------+-------------+------------+-------------+-----------+--------------+
CNO<0>                                       |        2.310|      SLOW  |        1.273|       FAST|         0.189|
CNO<1>                                       |        2.310|      SLOW  |        1.273|       FAST|         0.189|
CNO<2>                                       |        2.124|      SLOW  |        1.087|       FAST|         0.003|
CNO<3>                                       |        2.121|      SLOW  |        1.084|       FAST|         0.000|
CNO<4>                                       |        2.359|      SLOW  |        1.322|       FAST|         0.238|
CNO<5>                                       |        2.359|      SLOW  |        1.322|       FAST|         0.238|
CNO<6>                                       |        2.173|      SLOW  |        1.136|       FAST|         0.052|
CNO<7>                                       |        2.125|      SLOW  |        1.088|       FAST|         0.004|
CNO<8>                                       |        2.125|      SLOW  |        1.088|       FAST|         0.004|
CNO<9>                                       |        2.124|      SLOW  |        1.087|       FAST|         0.003|
CNO<10>                                      |        2.310|      SLOW  |        1.273|       FAST|         0.189|
CNO<11>                                      |        2.310|      SLOW  |        1.273|       FAST|         0.189|
CNO<12>                                      |        2.308|      SLOW  |        1.271|       FAST|         0.187|
CNO<13>                                      |        2.361|      SLOW  |        1.324|       FAST|         0.240|
CNO<14>                                      |        2.122|      SLOW  |        1.085|       FAST|         0.001|
CNO<15>                                      |        2.123|      SLOW  |        1.086|       FAST|         0.002|
CNO<16>                                      |        2.123|      SLOW  |        1.086|       FAST|         0.002|
---------------------------------------------+-------------+------------+-------------+-----------+--------------+


Timing summary:
---------------

Timing errors: 159  Score: 174879  (Setup/Max: 174879, Hold: 0)

```

```
Constraints cover 87304990 paths, 0 nets, and 81976 connections

Design statistics:
   Minimum period:  15.943ns{1}   (Maximum frequency:  62.723MHz)
   Minimum input required time before clock:   2.666ns
   Minimum output required time after clock:   2.364ns


------------------------------------Footnotes-----------------------------------
1)  The minimum period statistic assumes all single cycle delays.

Analysis completed Fri Aug  1 16:15:35 2025
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Trace Settings:
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Trace Settings

Peak Memory Usage: 856 MB
```